VMIVME-5550
Multidrop Reflective Memory with Interrupts

- High-speed, easy-to-use parallel network
- Data written to memory in one node is also written to memory in all nodes on the network
- Multidrop capability (up to 16 nodes)
- Data transferred at 20 Mbyte/s (50-foot cable)
- Any node on the network can generate an interrupt in any other node on the network or in all network chassis simultaneously
- No processor overhead
- No processor involvement in the operation of the network
- Up to 4 Mbyte of Reflective Memory
- Differential line drivers and receivers
- A24:A32:D32:D16:D8 memory access
- A24:A32:D8 status and control access
- Single 6U board

INTRODUCTION — VMIVME-5550 is a high-performance multidrop VME-to-VME network. Data is transferred by writing to on-board global RAM. The data is automatically sent to the location in memory on all Reflective Memory boards on the network (refer to Figure 1).

SPECIFICATIONS

Memory Size: 256 Kbyte, 512 Kbyte, 1 Mbyte, 2 Mbyte, or 4 Mbyte

Access Time:
360 ns (worst-case arbitration)
200 ns (best-case arbitration)

TRANSFER SPECIFICATION

Transfer Rate:
20 Mbyte/s (longword accesses)[1]
10 Mbyte/s (word accesses)[1]
5 Mbyte/s (byte accesses)[1]

COMPATIBILITY

This product complies with the VMEbus specification (ANSI/IEEE STD 1014-1987, IEC 821, and IEC 297), with the following mnemonics:

A32:A24:A16: D32/D16/D08 (EO):
Slave: 39/3D:09/0D
Form factor: 6U

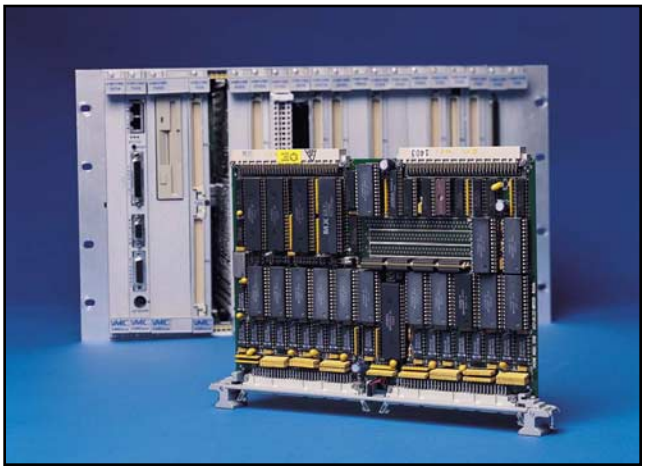
INTERCONNECTION

Cable Requirements: Two 64-conductor twist-n-flat ribbon cables. A wide variety of standard lengths are available.

Cable Length: 1,000 ft maximum

Configuration: Linear with up to 16 nodes

1. Network transfer rate with a total cable length of 5 feet.



POWER REQUIREMENTS

7.0 A maximum at +5 VDC

PHYSICAL/ENVIRONMENTAL

Temperature Range: 0 to 55 ˚C, operating
-40 to 85 °C, storage

Relative Humidity: 20 to 80 percent, noncondensing

MTBF: 104,500 hours (217F)

Ordering Options

June 18, 2001 800-005550-000 H	A	B	C	–	D	E	F
VMIVME-5550 –			0	–			

A = Memory Options
0 = 256 Kbyte
1 = 512 Kbyte
2 = 1 Mbyte
3 = 2 Mbyte
4 = 4 Mbyte

B = FIFO Option
0 = 512 Transfer FIFO
1 = 4 Kbyte Transfer FIFO

C = 0 (Option reserved for future use)

Connector Data

Compatible Connector	Panduit No. 120-964-435
Strain Relief	Panduit No. 100-000-072
PC Board Connector	Panduit No. 120-964-033A

Note

Panduit it also known as ITW/Pancon.

For Ordering Information, Call:
1-800-322-3616 or 1-256-880-0444 • FAX (256) 882-0859
E-mail: info@vmic.com Web Address: www.vmic.com

DATA TRANSFERS

Data written into the Reflective Memory is broadcast to all nodes on the network without further involvement of the sending or receiving nodes. Data is transferred from memory locations on the sending nodes to corresponding memory locations on the receiving nodes.

A functional block diagram of the VMIVME-5550 is shown in Figure 2.

PRODUCT OVERVIEW — The Reflective Memory concept provides a very fast and efficient way of sharing data across distributed VMEbus computer systems.

VMIC's VMIVME-5550 Reflective Memory interface allows data to be shared between up to 16 independent VMEbus systems (nodes) at rates up to 20 Mbyte/s. Each Reflective Memory board may be configured with 256 Kbyte to 4 Mbyte of on-board SRAM. The local SRAM provides fast Read access times to stored data. Writes are stored in local SRAM and broadcast over a high-speed parallel data bus to other Reflective Memory nodes. The transfer of data between nodes is software transparent, so no I/O overhead is required. Transmit and Receive FIFOs buffer data during peak data rates to optimize CPU and bus performance to maintain high data throughput.

The Reflective Memory also allows interrupts to one or more nodes by writing to a byte register.

These interrupt (three level, user definable) signals may be used to synchronize a system process, or used to follow any data that may have preceded it. The interrupt always follows the data to ensure the reception of the data before the interrupt is acknowledged.

1 Mbyte, 512 Kbyte, and 256 Kbyte VMIVME-5550 boards may be intermixed on the same link since all of these options pass a 1 Mbyte relative address across the link. The 4 and 2 Mbyte VMIVME-5550 boards should not be mixed with the 1 Mbyte, 512 Kbyte, or 256 Kbyte since they pass a 4 Mbyte relative address across the link. The 4 and 2 Mbyte VMIVME-5550 boards may be intermixed on the same link.

LINK ARBITRATION — Node addresses are set by on-board jumpers and may be read in the Status Register. Node 0 is the network arbiter. Control of the link is passed from the Node 0 to all other nodes on the network in a round robin fashion. As each node receives control of the link, it broadcasts all data written to its memory since the last time it had control of the link. This data is contained in the node's output buffer. After the entire contents of the output buffer is broadcast, control of the link is passed back to Node 0. Node 0 then broadcasts the contents of its output buffer and passes control to the next node on the link.

INTERRUPT TRANSFERS — In addition to transferring data between nodes, the VMIVME-5550 will allow any processor in any chassis to generate a VMEbus interrupt on any other chassis. These interrupts would generally be used to indicate to the receiving chassis that new data has been sent and is ready for processing. These interrupts are also used to indicate that processing of old data is completed and the receiving chassis is ready for new data.

Three interrupts are available. The user may define the function, priority, and vector for each interrupt. Any processor can generate an interrupt on any other VMEbus on the network on which the same interrupt is not already pending. In addition, any processor on the network can generate an interrupt on all VMEbuses on the network simultaneously. Interrupts are generated by simply writing to a single VMIVME-5550 register.

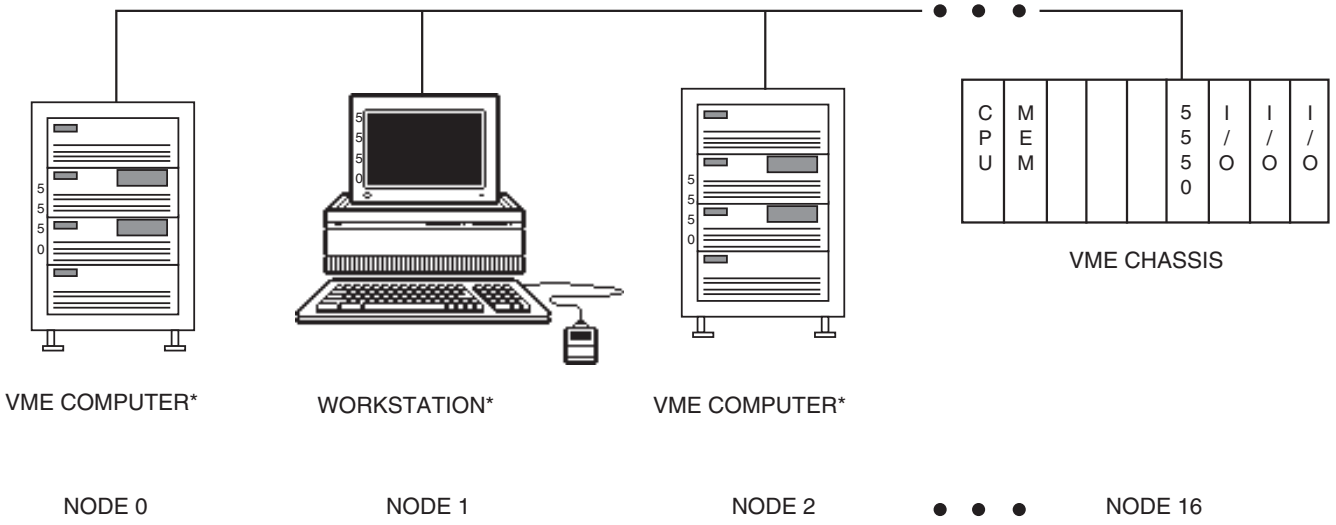
ERROR DETECTION AND RECOVERY — When Node 0 detects that there has been no activity on the link for more than 5 µs, it takes control of the link and passes control to the next node in the round robin sequence. As a result, node failures or nodes with power loss (except Node 0) will not prevent the link from operating.

It is possible for the output buffer to become full. An interrupt is available to signal the buffer is half full. A bit in a Status Register is also available to indicate when the buffer is full. The user can use any combination of the facilities to prevent overfilling the buffer. An attempt to write to the VMIVME-5550 memory when the output buffer is full will result in the generation of BERR to prevent data loss.

Table 1. Recommended Data Rate Versus Cable Length

Length (feet)	Data Rate Transfers/s (32-bit Cable Transfers)	Data Rate Bytes/s (32-bit Cable Transfers)
0 to 50	5 M longwords	20 Mbyte
50 to 100	2.5 M longwords	10 Mbyte
101 to 250	1.25 M longwords	5 Mbyte
251 to 1,000	.625 M longwords	2.5 Mbyte

TRADEMARKS



* Nodes can be VMEbus-based computers or computers with VMEbus I/O channels, such as Sun, Harris Night Hawk, Concurrent, Silicon Graphics, Data General, Motorola Delta Series, Encore 91 Series, and VMEbus chassis, etc.

Figure 1. Typical Network Using Reflective Memory

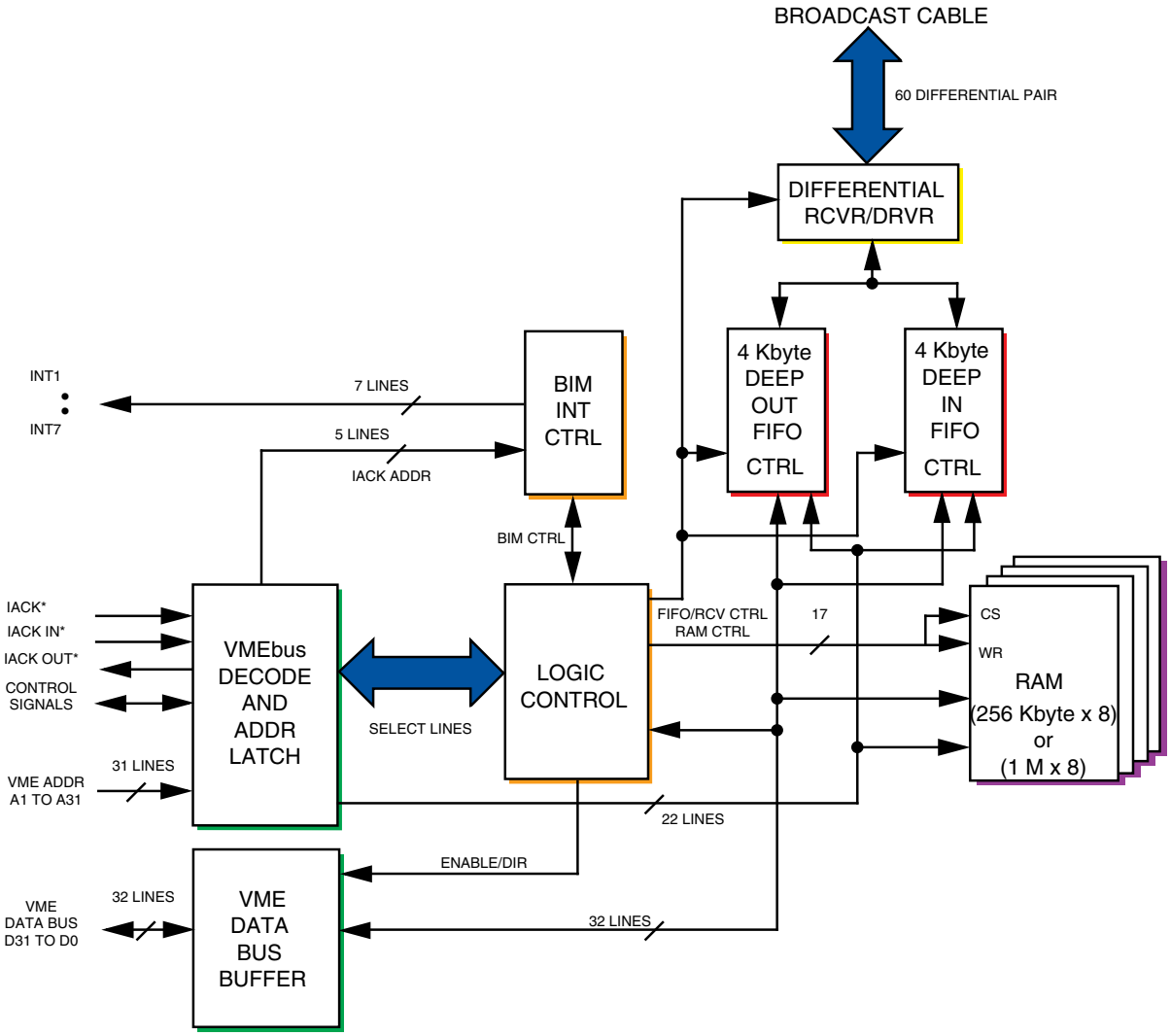


Figure 2. VMIVME-5550 Functional Block Diagram