VMIVME-5620
Intelligent HSD Emulator

- High-performance HSD interface designed to minimize host software overhead
- Executes commands from lists in memory
- IBL compatibility high or low priority
- HSD external mode support
- Data buffering (FIFOs)
- Data chaining and command chaining
- 68020 microprocessor
- Block transfers
- 32-bit DMA transfers over HSD bus
- 4 Mbyte/s transfer rate (VMIVME-5620 to VMIVME-5620)
- Programmable VMEbus address modifiers (as master)
- Programmable interrupt vectors and level
- HSD compatibility as HSD master or HSD slave
- VMEbus compatible (ANSI/IEEE STD 1014 - 1987 IEC 821 and 297)
- MA32: MBLT32 as VME master
- SAD024: SD32 as VMEbus slave
- VMEbus-to-VMEbus link using two boards
- 250-foot maximum cable length
- Front panel fail LED
- Jumper-selectable slave address
- Bus release: ROR, RWD, FAIR, RCLR
- Jumper-enabled system controller

INTRODUCTION — The VMIVME-5620 is an Encore HSD-compatible HSD emulator implemented on a double Eurocard. Two flat 50-conductor cables with socket connectors at both ends connect the VMIVME-5620 to the Encore HSD/IBL Interface or other HSD-compatible device.

The VMIVME-5620 uses an integrated VMEbus interface (Cypress VIC068), and an on-board local bus with processor and memory that interprets lists (IOCL) of host-based I/O Control Blocks (IOCBs). The VMEbus interface provides variable width host global memory access, and interrupts to the host interrupt handler. Figure 1 is a block diagram of the VMIVME-5620.

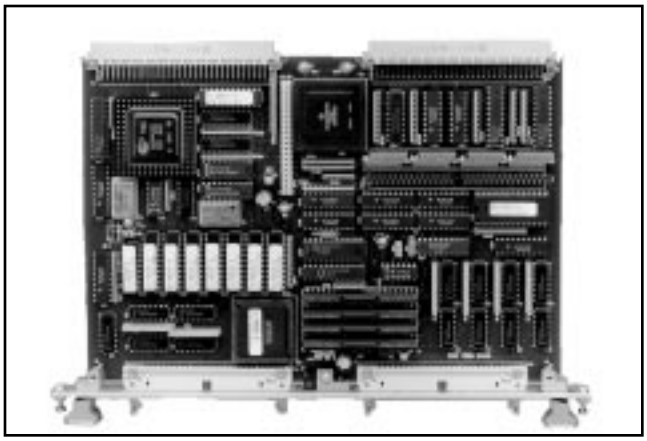
The VMIVME-5620 can function as either HSD master or HSD slave. However, the VMIVME-5620 is designed with features that make it particularly effective as an HSD master in minimizing host processor overhead. Listed below are some examples of system configurations in which the VMIVME-5620 may be used.

a. VMIVME-5620 as HSD master in a VME-based computer controlling Encore/Gould peripherals with an HSD interface (shown in Figure 2).

b. VMIVME-5620 as an HSD slave in a VME-based computer or embedded controller being driven by an HSD master in another computer (shown in Figure 3). The HSD master could be an Encore/Gould HSD on a SEL bus or another VMIVME-5620 in a VME-based computer.

c. VMIVME-5620 as HSD master in a VME-based computer interfaced via a VMIVME-HSDA to a VME-based embedded controller, such as the VMIC series of Intelligent I/O Controllers (IIOCs).

Some examples of computers that can be used with the VMIVME-5620 are: Encore Series 91, Concurrent, Silicon Graphics, Harris Night Hawk, DEC, Sun Workstations (Series 3 and 4), Modcomp, and Motorola Delta Series.



HSD MASTER MODE — The VMIVME-5620 can operate in the HSD master mode, which is the mode used to drive HSD peripherals. It fully implements this mode, sending External Function Commands to the HSD peripheral device, receiving device status, and transferring data blocks to or from the device, all by interpreting an IOCL in VMEbus global memory. Further, it supports External Mode, in which the HSD peripheral device controls addressing and data transfers to or from VMEbus global memory. See Figure 2.

INTERbus LINK (IBL) MODE — The VMIVME-5620 can operate in the INTERbus Link (IBL) mode. This mode permits two HSD-compatible controllers, one of which may be an Encore HSD controller, to form a high-speed link. The IBL mode reroutes some signals on the HSD interface so that a *crossed* cable is not necessary. See Figure 3.

DATA FIFOs — Data FIFOs are provided so that data transfers on the VMEbus may take place asynchronously with the data transfers on the cable. The data FIFOs are 512 transfers deep (2,048 bytes).

PROGRAMMING CONSIDERATIONS — The VMIVME-5620 operates as both VMEbus master and slave. As a slave, the board receives setup parameters from the host CPU. These setup parameters are written into Control Registers and provide information such as: interrupt vectors,

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interrupt levels, and an address that points to a location in global memory which contains the Input Output Control Blocks (IOCBs).

The IOCBs are lists of commands for the HSD to execute. It executes these commands without further involvement from the host CPU. The VMIVME-5620 functions as a VMEbus master to retrieve the IOCB commands and execute them.

The VMIVME-5620 supports *Command Chaining*, which allows the board to execute the next IOCB in the list after the current IOCB in execution is completed. Only after completion of the entire IOCB list *chain*, does the host CPU become involved again.

The VMIVME-5620 also supports *Data Chaining* which allows data to be transferred into or out of noncontiguous portions of memory.

VMEbus DATA TRANSFERS

Slave: SAD024:SD32 A24:A16:AD0:D32: D16: D8 (EO)
Addressable on 64-byte boundaries (jumpers)

Master: A32:MBLT32 A32:A24:A16:D32:D16:D8 (EO): BLT
Bus request level 0, 1, 2, or 3
Interrupt level and vectors programmable

Bus Grant Delay: 50 ns

Maximum Transfer Rates:
VMIVME-5620 to -5620: 4 Mbytes/sec (32 bits wide)[1]
VMIVME-5620 to -HSD: HSD dependent, maximum 3.2 Mbyte/s [1]

TRANSFER SPECIFICATIONS

Maximum Block Size: 256 Kbyte (16-bit transfer counter)

Transfer Width: 32, 16, or 8 bits per HSD cycle

Transfer Mode: Bidirectional half-duplex

Address Counters: 32-bit

Command/Control: From list in memory, D32 or D16 or D8 (EO) DMA

I/O Cables: Two 50-conductor (twisted pair flat-ribbon) (Cables not included) [2]

Maximum Cable Length: 250 ft

System Controller Mode (Must Be in Slot One of the Chassis): SYSCLK driver
Iack daisy-chain driver
Four-level Bus Arbiter (Round Robin or priority)
BERR time-out watchdog [3]

PHYSICAL/ENVIRONMENTAL

Temperature: 0 to 55 °C, operating
-20 to 85 °C, storage

Humidity: 20 to 80 percent relative, noncondensing

Altitude: Operation to 10,000 ft

Cooling: Forced air convection

Dimensions: Double height Eurocard (6U)
(160 mm x 233.35 mm)

Power Requirements: 3.5 A (typical) at +5 VDC
5.0 A (maximum)

TRADEMARKS

1. Transfer rates degrade as a function of cable length and operating mode and are a function of VMEbus memory speeds. Rates specified are with 25-foot cables, IBL or Master/Slave modes, Bus Capture or Block Transfer modes, and VMEbus global memory with 88 ns write access time and 240 ns read access time. (Average Read/Write access time of 164 ns.) Please refer to the Encore Technical Manual No. 35-329-132-000, or to VMIC Document 500-005620-000 (the VMIVME-5620 Product Manual) for details.

2. VMIC recommends the cables be high-quality twisted-pair with overall shield, for lengths greater than 50 feet.

3. The BERR watchdog times any bus master, but is available only when the VMIVME-5620 is in slot one as the system controller. The VMIVME-5620 provides no BERR watchdog function, even for the VMIVME-5620's own master cycles, if the VMIVME-5620 is not in slot one. The VMIVME-0300 is available for use with system controllers in which no BERR watchdog timer is available.

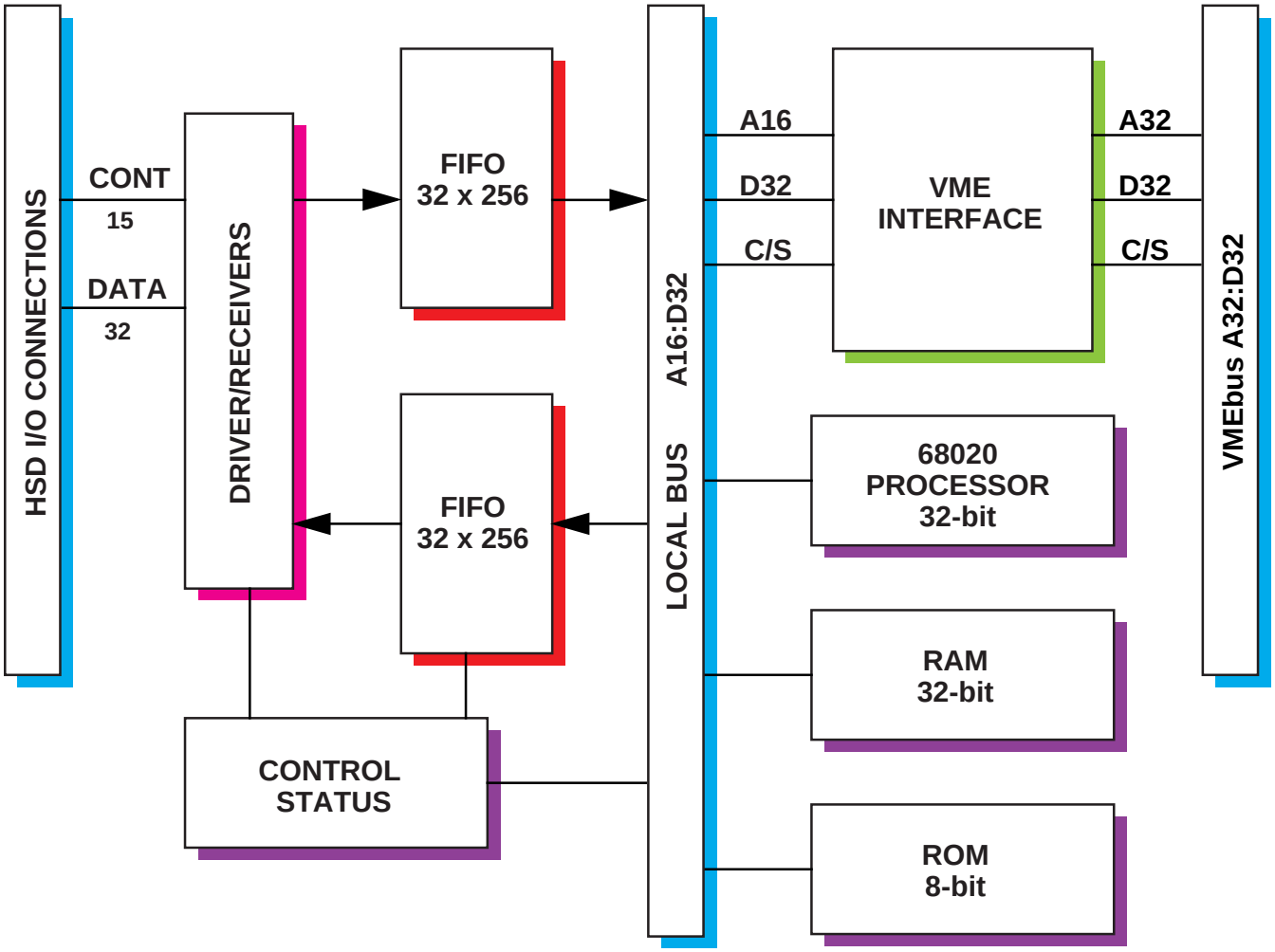

Figure 1. VMIVME-5620 Functional Block Diagram

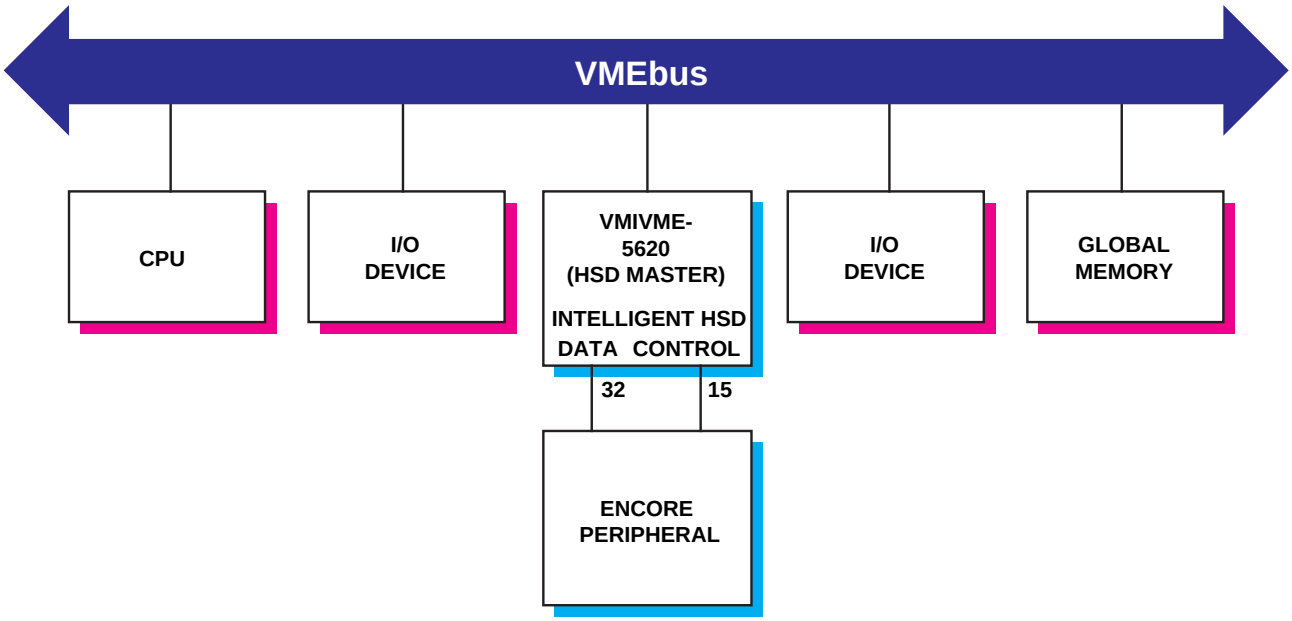

Figure 2. VMEbus System to Encore Peripheral

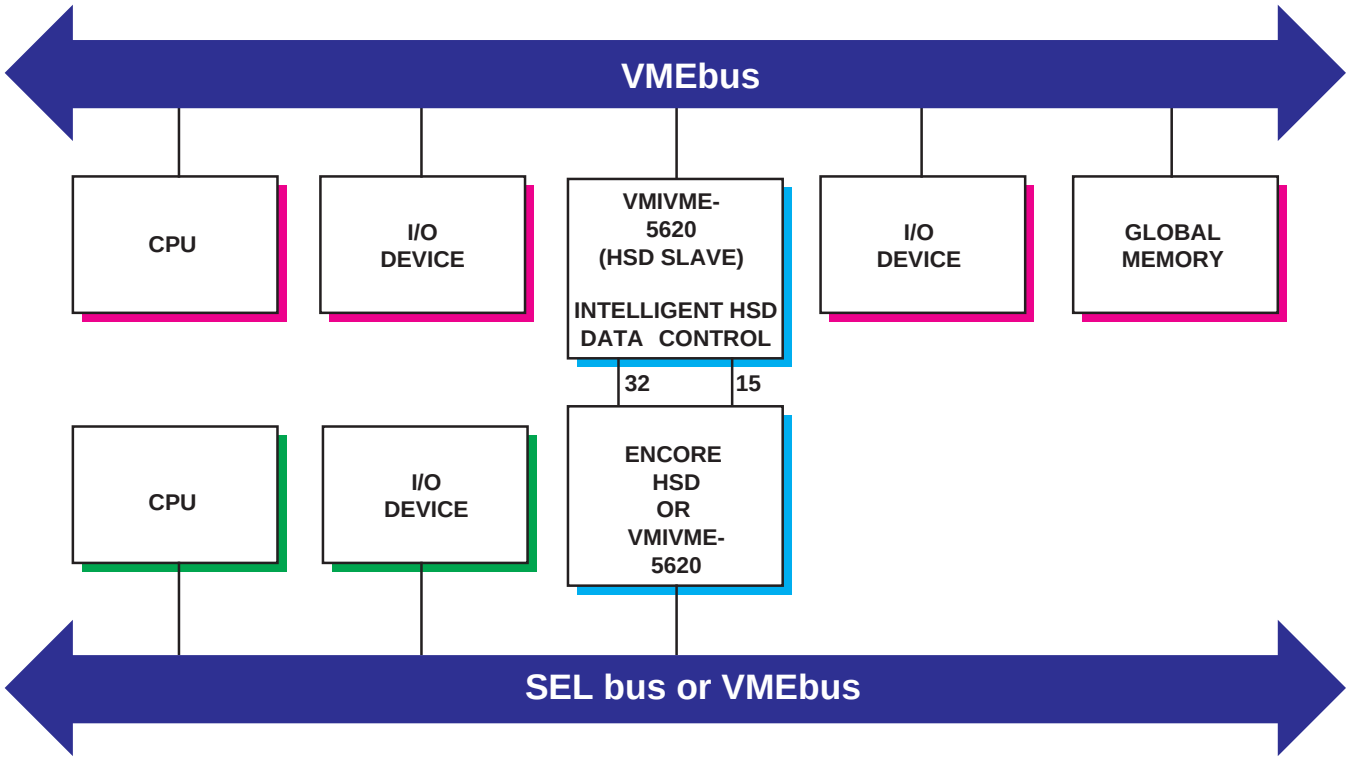

Figure 3. Encore to VMEbus System Block Diagram