AR-B9625
INDUSTRIAL GRADE
CPU BOARD
User's Guide

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0. PREFACE

0.1 COPYRIGHT NOTICE AND DISCLAIMER

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0.2 WELCOME TO THE AR-B9625 CPU BOARD

This guide introduces the Acrosser AR-B9625 CPU board.

The following information describes this card's functions, features, and how to start, set up and operate your AR-B9625. General system information can also be found here.

0.3 BEFORE YOU USE THIS GUIDE

If you have not already installed this AR-B9625, refer to the Chapter 3, "Setting Up The System" in this guide. Check the packing list, make sure the accessories are complete.

The AR-B9625 diskette provides the newest information about the card**. Please refer to the README.DOC file of the enclosed utility diskette**. It contains the modification, hardware & software information, and it has updates to product functions that may not be mentioned here.

0.4 RETURNING YOUR BOARD FOR SERVICE

If your board requires servicing, contact the dealer from whom you purchased the product for service information. If you need to ship your board to us for service, be sure it is packed in a protective carton. We recommend that you keep the original packaging for this purpose.

You can assure efficient servicing of your product by following these guidelines:

1. Include your name, address, daytime telephone and facsimile numbers and E-mail.
2. A description of the system configuration and/or software at the time of malfunction,
3. And a brief description of the symptoms.

0.5 TECHNICAL SUPPORT AND USER COMMENTS

User's comments are always welcome as they assist us in improving the usefulness of our products and the understanding of our publications. They form a very important part of the input used for product enhancement and revision.

We may use and distribute any of the information you supply in any way we believe appropriate without incurring any obligation. You may, of course, continue to use the information you supply.

If you have suggestions for improving particular sections or if you find any errors, please indicate the manual title and book number.

Please send your comments to Acrosser Technology Co., Ltd. or your local sales representative.

Internet electronic mail to: webmaster@acrosser.com

0.6 ORGANIZATION

This manual covers the following topics (see the Table of Contents for a detailed listing):

Chapter 1, "Overview", provides an overview of the system features and packing list.
Chapter 2, "System Controller" describes the major structure.
Chapter 3, "Setting Up the System", describes how to adjust the jumper, and the connector's settings.
Chapter 4, "CRT/LCD Flat Panel Display", describes the configuration and installation procedure using a LCD display.
Chapter 5, "Installation", describes setup procedures including information on the utility diskette.
Chapter 6, "BIOS Console", provides the BIOS options settings.
Chapter 7, Specifications
Chapter 8, Placement & Dimensions
Chapter 9, Programming RS-485 & Index

0.7 STATIC ELECTRICITY PRECAUTIONS

Before removing the board from its anti-static bag, read this section about static electricity precautions.
Static electricity is a constant danger to computer systems. The charge that can build up in your body may be more than sufficient to damage integrated circuits on any PC board. It is, therefore, important to observe basic precautions whenever you use or handle computer components. Although areas with humid climates are much less prone to static build-up, it is always best to safeguard against accidents that may result in expensive repairs. The following measures should be sufficient to protect your equipment from static discharge:
Touch a grounded metal object to discharge the static electricity in your body (or ideally, wear a grounded wrist strap).
When unpacking and handling the board or other system components, place all materials on an anti-static surface.
Be careful not to touch the components on the board, especially the "golden finger" connectors on the bottom of the board.

1. OVERVIEW

This chapter provides an overview of your system features and capabilities. The following topics are covered:

- Introduction
- Packing List
- Features

1.1 INTRODUCTION

The AR-B9625 is new generation half-size CPU board. This card offers much greater performance than the older cards, such as support for four RS-232C ports and one 168-pin DIMM socket for up to 128MB of extended memory SDRAM.

The unit also comes with a programmable watchdog timer and other standard interfaces. The CPU board is excellent for embedded systems, MMI's, workstations, medical applications or POS/POI systems.

The AR-B9625's on-board VGA, offers the most exciting possibilities yet to the industry. The on-board VGA/LCD controller brings about a whole new dimension in industrial computing. No longer do you have to worry about adding an extra card to your system.

1.2 PACKING LIST

Some accessories are included with the system. Before you begin installing your AR-B9625 board, take a moment to make sure that the following items have been included inside the AR-B9625 package.

- The quick setup manual
- 1 AR-B9625 all-in-one single CPU board
- 1 Hard disk drive interface cable
- 1 Parallel port interface cable
- 1 floppy interface cable
- 1 PS/2 mouse adapter
- Acrosser's AR-B9425 audio card
- 1 audio adapter cable
- 4 RJ-45 to DB-9 adapter
- 2 Software utility diskettes.

1.3 FEATURES

The system provides a number of special features that enhance its reliability, ensure its long-term availability, and improve its expansion capabilities, as well as its hardware structure.

- Cyrix GXM-200 MHz CPU (also compatible with other Cyrix GXM CPUs)
- On chip UMA-system VGA (On-board CRT and TFT-LCD panel display 800x600 LCD)
- Supports IDE hard disk drives
- Supports floppy disk drives
- Supports 1 bi-directional parallel port
- Supports 16-bit PnP sound system
- 100/10-Base2, shielded RJ-45 edge connector
- PC/AT compatible keyboard
- Programmable watchdog timer
- AWARD Flash BIOS
- Multi-layer PCB for noise reduction
- 4 COM ports: 1 of the 4 is switchable to RS-485/RS-232
- 1 of the 4 supports IrDA compatible transmissions
- Dimensions: 146.1mm X 203.2mm

2. SYSTEM CONTROLLER

This chapter describes the main structure of the AR-B9625 CPU board. The following topics are covered:

- Microprocessors
- DMA Controller
- Keyboard Controller
- Interrupt Controller
- Serial Port
- Parallel Port

2.1 MICROPROCESSOR

The AR-B9625 uses the Cyrix GXM-200 CPU (or other GXM CPUs), it is an advanced 64-bit x86 compatible processor offering high performance, fully accelerated 2D graphics, a 64-synchronous DRAM controller and a PCI bus controller, all on a single chip. This latest generation of the MediaGX processor enables a new class of premium performance notebook/desktop, and IPC computer designs.

The MediaGX MMX enhanced processor companion chips provide advanced video and audio functions and permit direct interface to memory. This high-performance 64-bit processor is x86 instruction set compatible and supports MMX technology.

This processor is the latest member of the Cyrix MediaGX family, offering high performance, fully accelerated 2D graphics, synchronous memory interface and a PCI bus controller, all on a single chip. As described in separate manuals, the Cx5520 and the Cx5530 I/O Companion chips fully enable the features of the MediaGX processor with MMX support. These features include full VGA and VESA video, 16-bit stereo sound, IDE interface, ISA interface, SMM power management, and AT compatibility logic. In addition, the newer Cx5530 provides an Ultra DMA/33 interface, MPEG2 assist, and is AC97 Version 2.0 audio compliant.

In addition to the advanced CPU features, the MediaGX processor integrates a host of functions which are typically implemented with external components. A full-function graphics accelerator provides pixel processing and rendering functions.

The Cyrix MediaGX MMX-Enhanced Processor represents a new generation of x86-compatible 64-bit microprocessors with sixth-generation features. The decoupled load/store unit (within the memory management unit) allows multiple instructions in a single clock cycle. Other features include single-cycle execution, single-cycle instruction decode, 16KB write-back cache, and clock rates up to 266MHz. These features are possible by the use of advanced-process technologies and superpipelining.

2.2 DMA CONTROLLER

The equivalent of two 8237A DMA controllers are implemented on the AR-B9625 board. Each controller is a four-channel DMA device that will generate the memory addresses and control signals necessary to transfer information directly between a peripheral device and memory. This allows high speed information transfer with less CPU intervention. The two DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1) and three channels for transfers to 16-bit peripherals (DMA2). DMA2 channel 0 provides the cascade interconnection between the two DMA devices, thereby maintaining IBM PC/AT compatibility.

The Following is the system information for the DMA channels:

Slave with four 8-bit chnls	**Master with three 16-bit chnls**
DMA Controller 1	**DMA Controller 2**
Channel 0: Spare	Channel 4(0): Cascade for controller 1
Channel 1: IBM SDLC	Channel 5(1): Spare
Channel 2: Diskette adapter	Channel 6(2): Spare
Channel 3: Spare	Channel 7(3): Spare

Table 1-1 DMA Channel Controller

2.3 KEYBOARD CONTROLLER

The 8042 processor is programmed to support the keyboard serial interface. The keyboard controller receives serial data from the keyboard, checks its parity, translates scan codes, and presents it to the system as a byte data in its output buffer. The controller can interrupt the system when data is placed in its output buffer, or wait for the system to poll its status register to determine when data is available.

Data can be written to the keyboard by writing data to the output buffer of the keyboard controller.

Each byte of data is sent to the keyboard controller in a series with an odd parity bit automatically inserted. The keyboard controller is required to acknowledge all data transmissions. Therefore, another byte of data will not be sent to keyboard controller until acknowledgment is received for the previous byte sent. The "output buffer full" interruption may be used for both send and receive routines.

2.4 INTERRUPT CONTROLLER

The equivalent of two 8259 Programmable Interrupt Controllers (PIC) are included on the AR-B9625 board. They accept requests from peripherals, resolve priorities on pending interrupts in service, issue interrupt requests to the CPU, and provide vectors which are used as acceptance indices by the CPU to determine which interrupt service routine to execute. These two controllers are cascaded with the second controller representing IRQ8 to IRQ15, which is rerouted through IRQ2 on the first controller.

The following is the system information of interrupt levels:

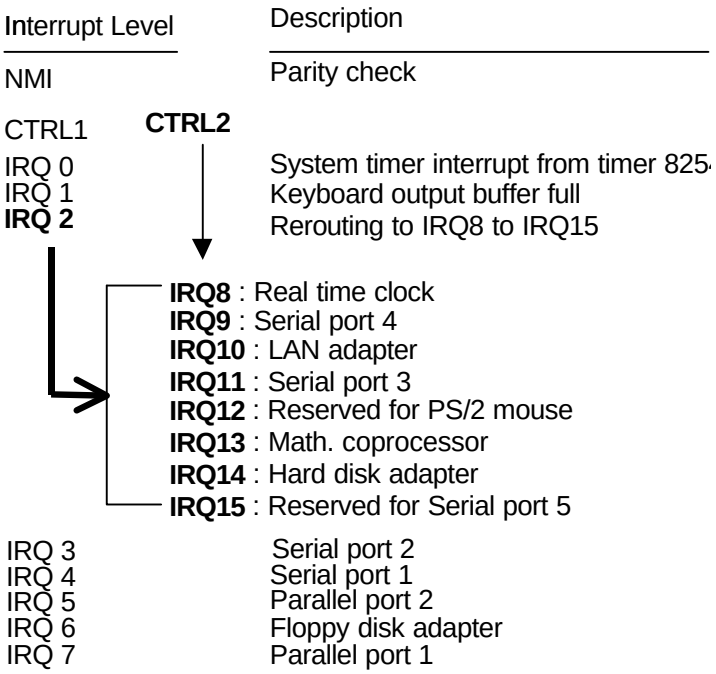


Figure 1-2 Interrupt Controller

2.4.1 I/O Port Address Map

Hex Range	Device
000-01F	DMA controller 1
020-021	Interrupt controller 1
022-023	Cyrix CX5530
040-04F	Timer 1
050-05F	Timer 2
060-06F	8042 keyboard/controller

Hex Range	Device
070-071	Real-time clock (RTC), non-maskable interrupt (NMI)
080-09F	DMA page registers
0A0-0A1	Interrupt controller 2
0C0-0DF	DMA controller 2
0F0	Clear Math Co-processor
0F1	Reset Math Co-processor
0F8-0FF	Math Co-processor
170-178	Fixed disk 1
1F0-1F8	Fixed disk 0
201	Game port
208-20A	EMS register 0
218-21A	EMS register 1
278-27F	Parallel printer port 2 (LPT 2)
2E8-2EF	Serial port 4 (COM 4)
2F8-2FF	Serial port 2 (COM 2)
300-31F	Prototype card/streaming type adapter
320-33F	LAN adapter
378-37F	Parallel printer port 1 (LPT 1)
380-38F	SDLC, bisynchronous
3A0-3AF	Bisynchronous
3B0-3BF	Monochrome display and printer port 3 (LPT 3)
3C0-3CF	EGA/VGA adapter
3D0-3DF	Color/graphics monitor adapter
3E8-3EF	Serial port 3 (COM 3)
3F0-3F7	Diskette controller
3F8-3FF	Serial port 1 (COM 1)

Table 1-2 I/O Port Address Map

2.4.2 Real-Time Clock and Non-Volatile RAM

The AR-B9625 contains a real-time clock compartment that maintains the date and time in addition to storing configuration information about the computer system. It contains 14 bytes of clock and control registers and 114 bytes of general purpose RAM. Because of the use of CMOS technology, it consumes very little power and can be maintained for long periods of time using an internal Lithium battery. The contents of each byte in the CMOS RAM are listed as follows:

Address	Description
00	Seconds
01	Second alarm
02	Minutes
03	Minute alarm
04	Hours
05	Hour alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Status register A
0B	Status register B
0C	Status register C
0D	Status register D
0E	Diagnostic status byte
0F	Shutdown status byte
10	Diskette drive type byte, drive A and B
11	Fixed disk type byte, drive C
12	Fixed disk type byte, drive D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2-byte CMOS checksum
30	Low actual expansion memory byte
31	High actual expansion memory byte
32	Date century byte
33	Information flags (set during power on)
34-7F	Reserved for system BIOS

Table 1-3 Real-Time Clock & Non-Volatile RAM

2.4.3 Timer

The AR-B9625 provides three programmable timers, each with a timing frequency of 1.19 MHz.

Timer 0 The output of this timer is tied to interrupt request 0. (IRQ 0)

Timer 1 This timer is used to trigger memory refresh cycles.

Timer 2 This timer provides the speaker tone.
Application programs can load different counts into this timer to generate various sound frequencies.

2.5 SERIAL PORT

The ACEs (Asynchronous Communication Elements ACE1 to ACE4) are used to convert parallel data to a serial format on the transmit side and convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, 1.5 (in a five-bit format only) or two stop bits(in a 6,7, or 8-bit format). The ACEs are capable of handling divisors of 1 to 65535, and produce a 16x clock for driving the internal transmitter logic.

Provisions are also included to use this 16x clock to drive the receiver logic. Also included in the ACE a completed MODEM control capability, and a processor interrupt system that may be software tailored to the computing time required to handle the communications link.

The following table is a summary of each ACE accessible register

DLAB	Port Address	Register
0	base + 0	Receiver buffer (read)
		Transmitter holding register (write)
0	base + 1	Interrupt enable
X	base + 2	Interrupt identification (read only)
X	base + 3	Line control
X	base + 4	MODEM control
X	base + 5	Line status
X	base + 6	MODEM status
X	base + 7	Scratched register
1	base + 0	Divisor latch (least significant byte)
1	base + 1	Divisor latch (most significant byte)

Table 1-4 ACE Accessible Registers

(1) Receiver Buffer Register (RBR)

Bit 0-7: Received data byte (Read Only)

(2) Transmitter Holding Register (THR)

Bit 0-7: Transmitter holding data byte (Write Only)

(3) Interrupt Enable Register (IER)

Bit 0: Enable Received Data Available Interrupt (ERBFI)
Bit 1: Enable Transmitter Holding Empty Interrupt (ETBEI)
Bit 2: Enable Receiver Line Status Interrupt (ELSI)
Bit 3: Enable MODEM Status Interrupt (EDSSI)
Bit 4: Must be 0
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(4) Interrupt Identification Register (IIR)

Bit 0: “0” if Interrupt Pending
Bit 1: Interrupt ID Bit 0
Bit 2: Interrupt ID Bit 1
Bit 3: Must be 0
Bit 4: Must be 0
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(5) Line Control Register (LCR)

Bit 0: Word Length Select Bit 0 (WLS0)
Bit 1: Word Length Select Bit 1 (WLS1)

WLS1	WLS0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: Number of Stop Bit (STB)
Bit 3: Parity Enable (PEN)
Bit 4: Even Parity Select (EPS)
Bit 5: Stick Parity
Bit 6: Set Break
Bit 7: Divisor Latch Access Bit (DLAB)

(6) MODEM Control Register (MCR)

Bit 0: Data Terminal Ready (DTR)
Bit 1: Request to Send (RTS)
Bit 2: Out 1 (OUT 1)
Bit 3: Out 2 (OUT 2)
Bit 4: Loop
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(7) Line Status Register (LSR)

Bit 0: Data Ready (DR)
Bit 1: Overrun Error (OR)
Bit 2: Parity Error (PE)
Bit 3: Framing Error (FE)
Bit 4: Break Interrupt (BI)
Bit 5: Transmitter Holding Register Empty (THRE)
Bit 6: Transmitter Shift Register Empty (TSRE)
Bit 7: Must be 0

(8) MODEM Status Register (MSR)

Bit 0: Delta Clear to Send (DCTS)
Bit 1: Delta Data Set Ready (DDSR)
Bit 2: Training Edge Ring Indicator (TERI)
Bit 3: Delta Receive Line Signal Detect (DSLSD)
Bit 4: Clear to Send (CTS)
Bit 5: Data Set Ready (DSR)
Bit 6: Ring Indicator (RI)
Bit 7: Received Line Signal Detect (RSLD)

(9) Divisor Latch (LS, MS)

	LS	MS
Bit 0:	Bit 0	Bit 8
Bit 1:	Bit 1	Bit 9
Bit 2:	Bit 2	Bit 10
Bit 3:	Bit 3	Bit 11
Bit 4:	Bit 4	Bit 12
Bit 5:	Bit 5	Bit 13
Bit 6:	Bit 6	Bit 14
Bit 7:	Bit 7	Bit 15

Desired Baud Rate	Divisor Used to Generate 16x Clock
300	384
600	192
1200	96
1800	64
2400	48
3600	32
4800	24
9600	12
14400	8
19200	6
28800	4
38400	3
57600	2
115200	1

Table 2-1 Serial Port Divisor Latch

2.6 PARALLEL PORT

(1) Register Address

Port Address	Read/Write	Register
base + 0	Write	Output data
base + 0	Read	Input data
base + 1	Read	Printer status buffer
base + 2	Write	Printer control latch

Table 2-1 Registers' Address

(2) Printer Interface Logic

The parallel port of the NSPC87309 is for attaching various devices that accept eight bits of parallel data at standard TTL level.

(3) Data Swapper

The system microprocessor can read the contents of the printer's Data Latch through the Data Swapper by reading the Data Swapper address.

(4) Printer Status Buffer

The system microprocessor can read the printer status by reading the address of the Printer Status Buffer. The bit definitions are described as follows:

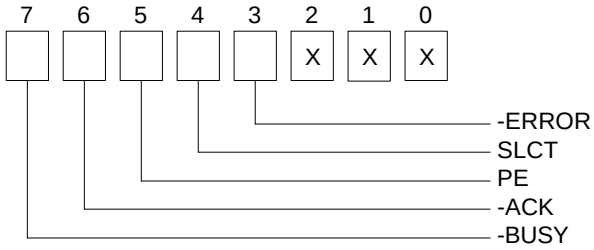


Figure 2-1 Printer Status Buffer

NOTE: X presents not used.

Bit 7: This signal may become active during data entry, when the printer is off-line during printing, or when the print head is changing position or in an error state. When Bit 7 is active, the printer is busy and can not accept data.

Bit 6: This bit represents the current state of the printer's ACK signal. A0 means the printer has received the character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before receiving a BUSY message stops.

Bit 5: A1 means the printer has detected the end of the paper.

Bit 4: A1 means the printer is selected.

Bit 3: A0 means the printer has encountered an error condition.

(5) Printer Control Latch & Printer Control Swapper

The system microprocessor can read the contents of the printer control latch by reading the address of printer control swapper. Bit definitions are as follows:

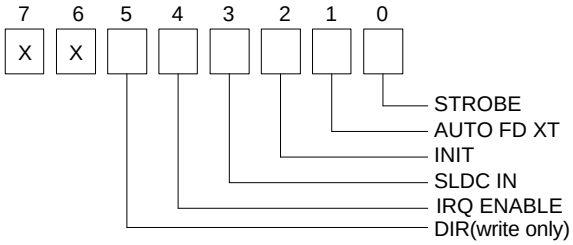


Figure 2-2 Bit's Definition

NOTE: X presents not used.

Bit 5: Direction control bit. When logic 1, the output buffers in the parallel port are disabled allowing data driven from external sources to be read; when logic 0, they work as a printer port. This bit is write only.

Bit 4: A1 in this position allows an interrupt to occur when ACK changes from low state to high state.

Bit 3: A1 in this bit position selects the printer.

Bit 2: A0 starts the printer (50 microseconds pulse, minimum).

Bit 1: A1 causes the printer to line-feed after a line is printed.

Bit 0: A0.5 microsecond minimum highly active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.

3. SETTING UP THE SYSTEM

This section describes pin assignments for the system's external connectors and the jumper settings.

- Overview
- System Setting

3.1 OVERVIEW

The AR-B9625 is an all-in-one Cyrix GXM-200 CPU board. This section provides the hardware's jumper settings, the connectors' locations, and the pin assignments. The #1 pin assignments have all been designed on the right side of the board with a "block" indication on the diagram.

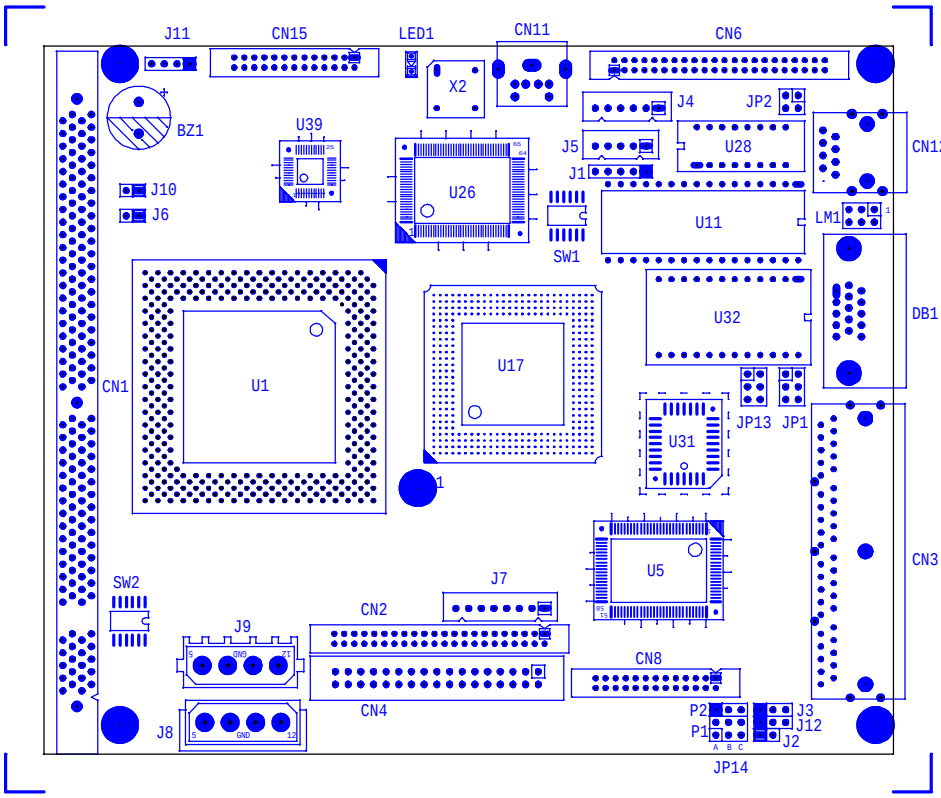


Figure 3-1 External System Location

3.2 SYSTEM SETTING

Jumper pins allow you to set specific system parameters. Set them by changing the pin location of jumper blocks. (A jumper block is a small plastic-encased conductor that slips over the pins.) To change a jumper setting, remove the jumper from its current location with your fingers or small needle-nosed pliers. Place the jumper over the two pins designated for the desired setting. Press the jumper evenly onto the pins. Be careful not to bend the pins.

We will show the locations of the AR-B9625 jumper pins, and the factory-default settings in <3.2.6> to <3.2.12> below.

CAUTION: Do not touch any electronic components unless you are safely grounded. Wear a grounded wrist strap or touch an exposed metal part of the system unit chassis. The static discharges from your fingers can permanently damage electronic components.

3.2.1 Keyboard Connector

(1) 6-Pin Mini DIN Keyboard Connector (CN11)

CN11 is a Mini-DIN 6-pin connector. This keyboard connector is a standard PS/2 type keyboard connector. This connector can also be used with a standard IBM-compatible keyboard when used in unison with the keyboard adapter cable included.

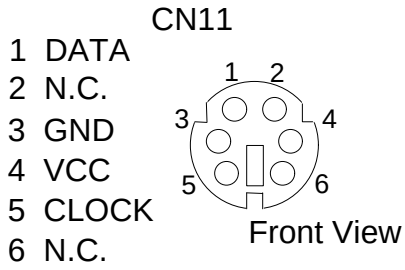


Figure 3-2 CN11: 6-Pin Mini Din Keyboard Connector

(2) AUX. Keyboard Connector (J5)

A PC/AT compatible keyboard can be used by connecting the provided adapter cable between the J5 connector and the keyboard. The pin assignments of the J5 connector are as follows:

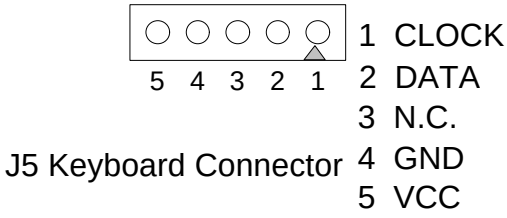


Figure 3-3 J5: AUX. Keyboard Connector

3.2.2 PS/2 Mouse Connector (J4)

To use a PS/2 mouse, an adapter cable(included) needs to be connected to the J4 (6-pin header type) connector. This adapter cable is mounted on a bracket and is included in your AR-B9625 package. The connector for the PS/2 mouse is a Mini-DIN 6-pin connector. Pin assignments for the PS/2 port connector are as follows:

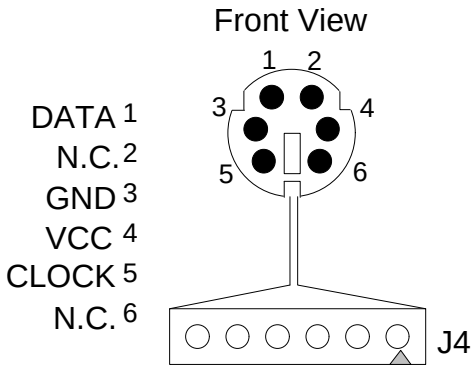


Figure 3-4 J4: PS/2 Mouse Connector

3.2.3 Hard Disk (IDE) Connector (CN6)

A 44-pin header type connector (CN6) is provided to interface with up to two embedded hard disk drives (IDE AT bus). This interface, through a 44-pin cable, allows the user to connect up to two drives in a "daisy chain" fashion. To enable or disable the hard disk controller, please use the BIOS Setup program, which is explained further in section <6.6>. The following table illustrates the pin assignments of the hard disk drive's 44-pin connector. The last pin on the cable is the master.

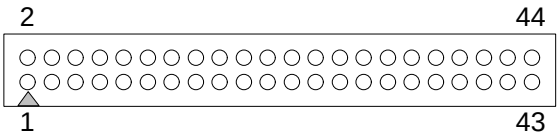


Figure 3-5 CN6: Hard Disk (IDE) Connector

Pin	Signal	Pin	Signal
1	-RESET	2	GROUND
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DATA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14
17	DATA 0	18	DATA 15
19	GROUND	20	NOT USED
21	IDEDREQ	22	GROUND
23	-IOW A	24	GROUND
25	-IOR A	26	GROUND
27	IDEIORDYA	28	GROUND
29	-DACKA	30	GROUND
31	AINT	32	GROUND
33	SA 1	34	Not Used
35	SA 0	36	SA 2
37	CS 0	38	CS 1
39	HD LED A	40	GROUND
41	VCC	42	VCC
43	GROUND	44	Not Used

Table 3-1 CN6: Hard Disk (IDE) Connector

3.2.4 FDD Port Connector (CN4)

The AR-B9625 provides a 34-pin header type connector for supporting up to two floppy disk drives in a daisy chain style. The last connector on the cable is the master.

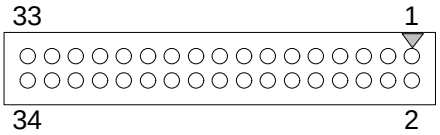


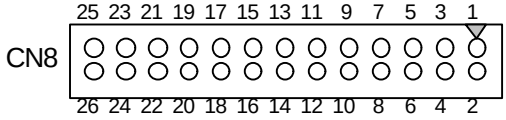
Figure 3-6 CN4: FDD Port Connector

Pin	Signal	Pin	Signal
1-33 (odd)	GROUND	18	-DIRECTION
2	-REDUCED WRITE CURRENT	20	-STEP OUTPUT PULSE
4	NOT USED	22	-WRITE DATA
6	NOT USED	24	-WRITE ENABLE
8	-INDEX	26	-TRACK 0
10	-MOTOR ENABLE A	28	-WROTE PROTECT
12	-DRIVE SELECT B	30	-READ DATA
14	-DRIVE SELECT A	32	-SIDE 1 SELECT
16	-MOTOR ENABLE B	34	-DISK CHANGE

Table 3-2 CN4: FDD Port Connector

3.2.5 Parallel Port Connector (CN8)

To use the parallel port, an adapter cable has been connected to the CN8 (26-pin header type) connector. This adapter cable is mounted on a bracket and is included in your AR-B9625 package. The connector for the parallel port is a 25 pin D-type female connector.



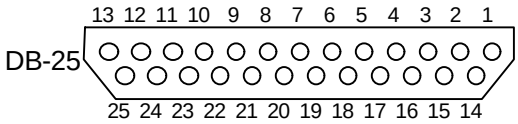


Figure 3-7 CN8: Parallel Port Connector

CN8	DB-25	Signal	CN8	DB-25	Signal
1	1	-Strobe	2	14	-Auto Form Feed
3	2	Data 0	4	15	-Error
5	3	Data 1	6	16	-Initialize
7	4	Data 2	8	17	-Printer Select In
9	5	Data 3	10	18	Ground
11	6	Data 4	12	19	Ground
13	7	Data 5	14	20	Ground
15	8	Data 6	16	21	Ground
17	9	Data 7	18	22	Ground
19	10	-Acknowledge	20	23	Ground
21	11	Busy	22	24	Ground
23	12	Paper	24	25	Ground
25	13	Printer Select	26	--	Not Used

Table 3-3 Parallel Port Pin Assignments

3.2.6 Serial Port

(1) Full RS-232 Signal / Power Select for COM-A (JP1)

The JP1 can be used to select the full RS-232 signal or a power select for COM A. If the user chooses the power supported version then the COM A's RTS will be used instead of the +12VDC signal; and the COM A's CTS used will be instead of the +5VDC signal.

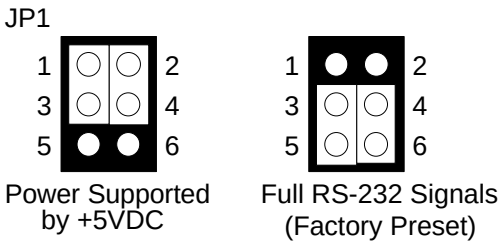


Figure 3-8 JP1: Full RS-232 Signal / Power Select for COM-A

(2) Full RS-232 Signal / Power Select for COM-B (JP13)

The JP13 can be used to select the full RS-232 signal or a power select for COM B. If the user chooses the power supported version then the COM B's RTS will be used instead of the +12VDC signal; and the COM B's CTS used will be instead of the +5VDC signal.

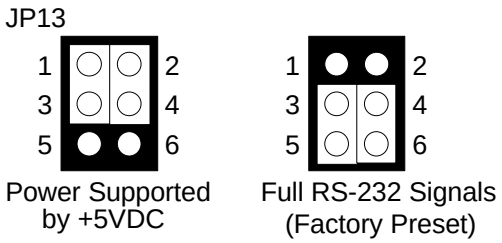


Figure 3-9 JP13: Full RS-232 Signal / Power Select for COM-B

(3) RS-232/RS-485 Select for COM-C (JP14)

The JP14 jumper is used to choose between the use of the on-board RS-232 or RS-485 for the CN3 – COM C. This can be used with the Acrosser (AR-M9912) RS-232/485 adapter without adding an outside power source.

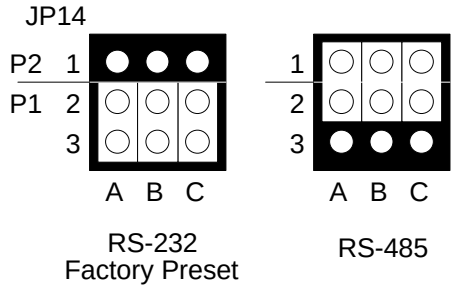


Figure 3-10 JP14: RS-232/RS-485 Select for COM-C

(4) RS-485 Terminator Select (J2)

When there is only one line the setting should be left off, but if you are using multiple blocks on a single line this should be set to "ON" in order to properly terminate the connection for better transmission of data.

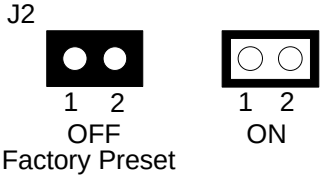


Figure 3-11 J2: RS-485 Terminator Select

(5) RS-232 Signal Header for COM C (J3)

This is an optional connection for COM C (RS-232). One line for transmission, one for reception and another for ground.

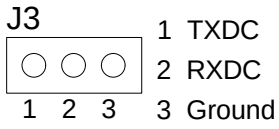


Figure 3-12 J3: RS-232 Signal Header for COM C

(6) RS-232 Signal Header for COM D (J12)

This is an optional connection for COM D (RS-232). One line for transmission, one for reception and another for ground.

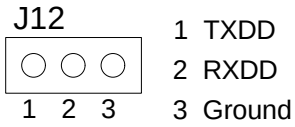


Figure 3-13 J12: RS-232 Signal Header for COM D

(7) RS-232C Connector (CN3)

There are four serial ports with EIA RS-232C interface on the AR-B9625. COM A, COM B and COM D use three on-board serial port Phone-Jack 10-pin female connectors. (CN3) is located at the right top side of the card. To configure these four serial ports, use the BIOS Setup program (covered later in section <6.6>). COM C can be adjusted by the jumpers on P1 & P2 for choosing between RS-485 and RS-232C.

The pin assignments of the CN3 connector for serial ports A, B, C & D are as follows:

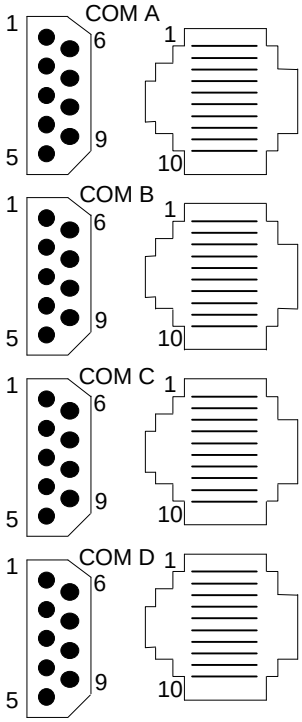


Figure 3-14 CN3: RS-232C Connector

CN3-A	DB-9	Signal	CN3-A	DB-9	Signal
1	1	-DCD	2	8	-CTS / +5V
3	7	-RTS / +5V	4	6	-DSR
5	2	RXD	6	3	TXD
7	4	-DTR	8	5	GND
9	5	GND	10	9	-RI

Table 3-4 Serial Port RS-232 COM A Pin Assignment

CN3-B	CN3-C	DB-9	Signal	CN3-B	CN3-C	DB-9	Signal
1	1	1	-DCD	2	2	8	-CTS
3	3	7	-RTS	4	4	6	-DSR
5	5	2	RXD	6	6	3	TXD
7	7	4	-DTR	8	8	5	GND
9	9	5	GND	10	10	9	-RI

Table 3-5 Serial Port RS-232 COM B & C Pin Assignment

CN3-D	DB-9	Signal	CN3-D	DB-9	Signal
1	1	-DCD	2	8	-CTS
3	7	-RTS / 485N+	4	6	-DSR
5	2	RXD	6	3	TXD
7	4	-DTR / 485N-	8	5	GND
9	5	GND	10	9	-RI

Table 3-6 Serial Port RS-232/RS-485 COM D Pin Assignment

(8) IrDA Header (J1)

When using the internal IrDA header it will automatically become COM D. This means that COM D will not be able to be used as a serial connection. This selection should be selected in the BIOS (The best setting is to use “Auto”).

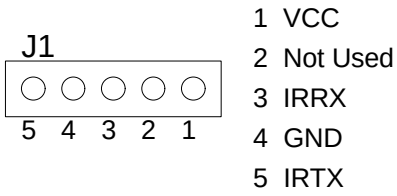


Figure 3-15 J1: IrDA Header

3.2.7 Network Setting

(1) Transferring Speed LED Header (JP2)

This LED presents the network transferring speed. If the speed is 100Mbps the LED is lit, and the speed is 10Mbps the LED is off.

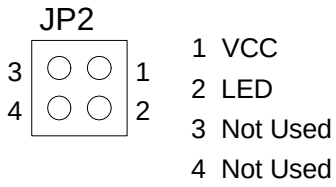


Figure 3-16 JP2: Transferring Speed LED Header

(2) RJ-45 Connector (CN12)

The CN12 connects the RJ-45 header, it' s the standard network header. The following table is CN12 pin assignment.

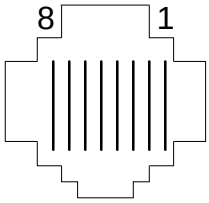


Figure 3-17 CN12: RJ-45 Connector

PIN (CN12)	FUNCTION
1	TPTX+
2	TPTX -
3	TPRX+
4	Not Used
5	Not Used
6	TPRX -
7	Not Used
8	Not Used

Table 3-7 RJ-45 Pin Assignment

3.2.8 Reset Header (J6)

The J6 is used to connect to an external reset switch. Shorting these two pins will reset the system.

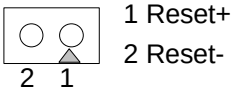


Figure 3-18 J6: Reset Header

3.2.9 External Speaker Header (J11)

Besides the on-board buzzer, you can use an external speaker by connecting directly to the J11 header.

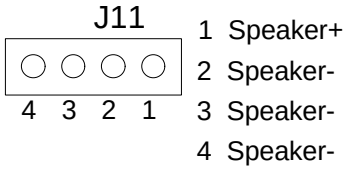


Figure 3-19 J11: External Speaker Header

3.2.10 26-Pin Audio Connector (CN15)

The CN15 is used to connect to a harness which has a D-SUB game and midi input, a line in, a line out, and a microphone. This cable harness adapter (AR-B9425) comes with the board.

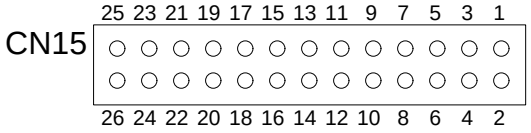


Figure 3-20 CN15: 26-Pin Audio Connector

PIN (CN15)	Signal	PIN (CN15)	Signal
1	CDINL	2	LININL
3	CDINR	4	LININR
5	VCC	6	Not Used
7	LINOUTL	8	MICIN
9	LINOUTR	10	PCBEEP
11	GND	12	GND
13	Not Used	14	Not Used
15	GND	16	GND
17	Not Used	18	Not Used
19	Not Used	20	Not Used
21	Not Used	22	Not Used
23	Not Used	24	Not Used
25	GND	26	GND

Table 3-8-Pin Audio Connector

Note: the connector does not contain the GAME (MIDI) port signal. When AR-B9425 audio card is used with this CPU board, the GAME port function is not supported.

3.2.11 Power Connector (J7 & J8)

The J8 is a 4-pin power connector and J7 is an 8-pin power connector. Using the J7, you can connect the power supply to the on board power connector for stand alone applications directly. Both J8 and J7 are standard connectors on all Acrosser boards, but the use of one or another is left to the discrepancy of the user.

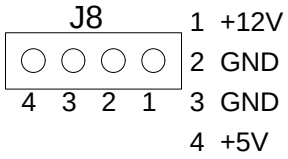


Figure 3-21 J8: 4-Pin Power Connector

The 8-pin J8 adds negative voltages for special applications.

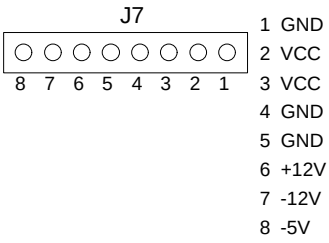


Figure 3-22 J7: 8-Pin Power Connector

3.2.12 CPU Select

(1) System Base Clock & CPU Clock Multiplier (SW1)

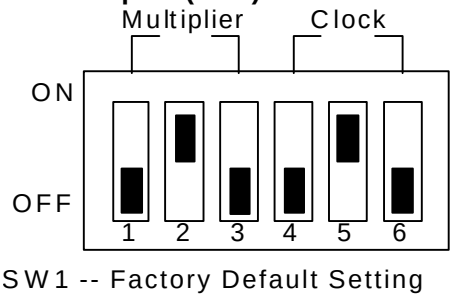


Figure 3-23 SW1: System Base Clock & CPU Clock Multiplier

(A) CPU Clock Multiplier Select (SW1)

The CPU clock is multiplied by the PCI clock and not by base clock. The PCI clock is set at 33.3MHz (as mentioned below) and can not be changed. This means that the 200MHz CPU will be set at "6X" and that a 300MHz GXM CPU would be set at "9X".

SW1-1	SW1-2	SW1-3	Multiplier	Note
ON	ON	ON	4X	
ON	ON	OFF	10X	
ON	OFF	ON	9X	300MHz
ON	OFF	OFF	5X	
OFF	ON	ON	Reserved	
OFF	ON	OFF	6X	Factory Preset
OFF	OFF	ON	7X	233MHz
OFF	OFF	OFF	8X	266MHz

Table 3-8 SW1: CPU Clock Multiplier

(B) CPU Base Clock Select (SW1)

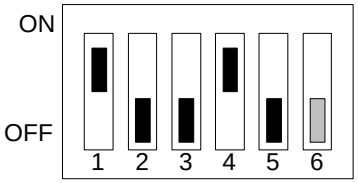
This board supports different types of GXM CPUs. The clock generator needs to be set on the fourth, fifth, and sixth switches of SW1.
The default setting, which is unchangeable) is set at the 33.3MHz PCI clock.

SW1-4	SW1-5	SW1-6	Base Clock	PCI Clock
ON	ON	OFF	25MHz	25MHz
OFF	ON	OFF	33.3MHz	33.3MHz
ON	OFF	OFF	30MHz	30MHz
OFF	OFF	OFF	27.5MHz	27.5MHz
ON	ON	ON	25.6MHz	25.6MHz
OFF	ON	ON	34.2MHz	34.2MHz
ON	OFF	ON	30.8MHz	30.8MHz
OFF	OFF	ON	37.5MHz	37.5MHz

Table 3-9 SW1: CPU Base Clock

(2) CPU Logic Core Voltage Select (SW2)

This board uses the Cyrix GXM-200 CPU, so it is recommended that the user leave the setting on the factory preset. Don't change the setting from the 2.86V setting because the CPU would then stop working. This is the setting for all GXM CPUs which an be used with this board.



SW2 -- Factory Default Setting

Figure 3-24 SW2: CPU Logic Core Voltage

SW2-1	SW2-2	SW2-3	SW2-4	SW2-5	SW2-6	Voltage
OFF	ON	OFF	OFF	OFF	--	2.16V
ON	ON	OFF	OFF	OFF	--	2.26V
ON	OFF	OFF	ON	OFF	--	2.86V
OFF	ON	OFF	ON	OFF	--	2.96V
OFF	ON	ON	ON	OFF	--	3.36V
ON	ON	ON	ON	OFF	--	3.46V

Table 3-13-10 SW2: CPU Logic Core Voltage

(3) CPU Power Header (J9)

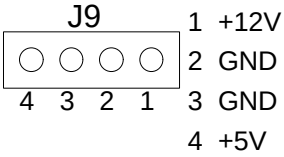


Figure 3-25 J9: CPU Power Header

(4) CPU Cooling Fan Power Header (J10)

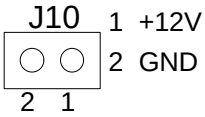


Figure 3-26 J10: CPU Cooling Fan Power Header

(5) Cyrix GX 200 setting

CPU	SW1 1-3 (Multiplier 6X)			SW1 4-6 (Base CLK.: 33.3 MHz)			SW2 1-5 (Logic Core Voltage: 2.96V)				
GX-200	1	2	3	4	5	6	1	2	3	4	5
	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	ON	OFF

4. CRT/LCD FLAT PANEL DISPLAY

This chapter describes the configuration and installation procedure using LCD and CRT displays. Both CRT and LCD displays may be used at the same time. Only TFT type LCDs may be used. CRT monitors should work with no problem under Windows 95/98. However, each type of LCD requires a different BIOS.

LCD Flat Panel Display
CRT & LCD Display

4.1 LCD FLAT PANEL DISPLAY

Each model of LCD requires different BIOS in order to work properly. If you want to use a panel that your board was not originally designed for then you can follow one of two procedures. If the BIOS you need is not on our website www.acrosser.com, then you can send us a sample of the panel you will be using and we will send it back to you with the new BIOS. Or, you can go through the process of getting the new BIOS on your own.

The second option would involve:

1. Downloading Cyrix' s LCD modifying utility <Panel.exe> from www.acrosser.com,
2. Use Panel.exe to adjust the "Timing"
   2.1 The timing variables should be adjusted till the LCD has the best possible qualities.
   2.2 The variables for timing will include the clock frequency, HTotal, FP VSYNC start and and, CRT HSYNC start and end, VTotal, FP VSYNC start and end, and the CRT VSYNC start and end.
3. These new LCD settings need to be sent to the technical support section of Acrosser.
4. Acrosser will then find the new register values and send them to Award BIOS for new BIOS,
5. Lastly, the new BIOS will be downloadable from our website upon completion.

Use the Flash Memory Writer utility to download the new BIOS file into the ROM chip to configure the BIOS default setting for different types of LCD panel. And then set your system properly and configure the AR-B9625 VGA module for the right type of LCD panel you are using.

The sample LCD models listed on the table at www.acrosser.com are just some of the LCD panel models. If you are using a different LCD panel other than those listed, contact Acrosser' s technical support department for help.

The following shows the block diagram of using AR-B9625 for LCD display.

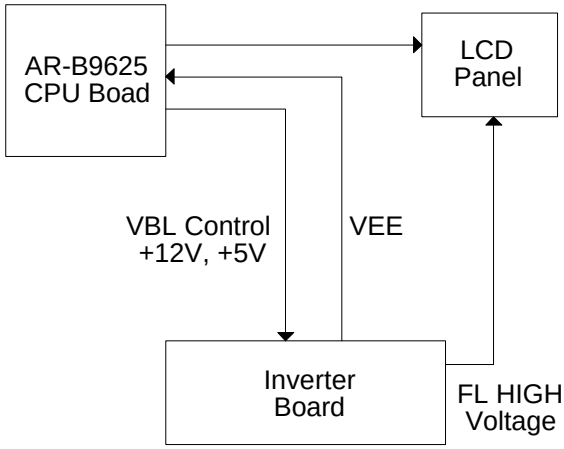


Figure 4-1 LCD Panel Block Diagram

The block diagram shows that AR-B9625 still needs components to be used with a LCD panel. The transfer board (AR-B9413) provides the control for the brightness and the contrast of the LCD panel while inverter board (AR-B9416) is the one that supplies the high voltage to drive the LCD panel. Both AR-B9413 and AAR-B9416 are available from Acrosser with all the necessary cables.

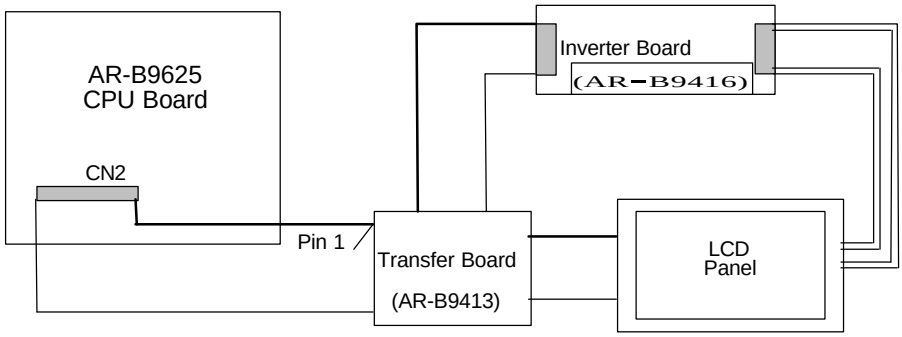


Figure 4-2 LCD Panel Cable Installation Diagram

NOTE: Be careful with the pin orientation when installing connectors and the cables. A wrong connection can easily destroy your LCD panel. The pin 1 of the cable connectors is indicated with a sticker and the pin1 of the ribbon cable usually has a different color.

4.2 CRT & LCD DISPLAY

The AR-B9625 supports a CRT colored monitor and a TFT LCD (DSTN LCDs are not supported with this board). It can be connected to create a compact video solution for the industrial environment. 1MB of RAM on-boarded allows a maximum CRT resolution of 1024X768 with 64K colors and a LCD resolution of 800X600 with 64K colors. Different VGA display modes are possible, but your monitor must possess certain characteristics (different modes require different drivers to display the mode desired.

4.2.1 CRT Connector (DB1)

DB1 is used to connect with a VGA monitor when you are using the on-board VGA controller as the display adapter. Pin assignments for the DB1 connector are as follows:

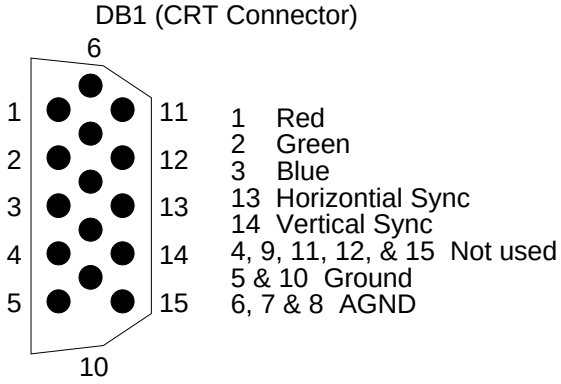


Figure 4-3 DB1: CRT Connector

4.2.2 LCD Panel Display Connector (CN2)

You may attach a display panel connector to this 44-pin connector with pin the assignments as shown below:

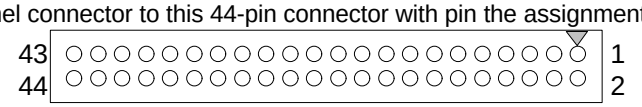


Figure 4-4 CN2: LCD Display Connector

Pin	Signal	Pin	Signal
1	GND	2	CLK
3	GND	4	HSYNCR
5	VSYNCR	6	GND
7	Not Used	8	Not Used
9	FPDR0	10	FPDR1
11	FPDR2	12	FPDR3
13	GND	14	FPDR4
15	FPDR5	16	Not Used
17	Not Used	18	FPDR6
19	FPDR7	20	GND
21	FPDR8	22	FPDR9
23	FPDR10	24	FPDR11
25	Not Used	26	Not Used
27	GND	28	FPDR12
29	FPDR13	30	FPDR14
31	FPDR15	32	FPDR16
33	FPDR17	34	GND
35	VCC	36	VCC
37	+12V	38	+12V
39	GND	40	GND
41	DISPENR	42	GKLENR
43	GND	44	VDDEN

Table 4-1 LCD Display Assignments

5. INSTALLATION

This chapter describes the installation procedure. The following topics are covered:

- Overview
- Utility Diskettes
- Watchdog Timer

5.1 OVERVIEW

This chapter provides information for you to set up a working system based on the AR-B9625 CPU board. Please carefully read the details of the CPU board's hardware descriptions before installation. Pay special attention to the jumper settings, switch settings and cable connections.

Follow steps listed below for proper installation:

Step 1 : Read the CPU board's hardware description in this manual.

Step 2 : Set jumpers.

Step 3 : Make sure that the power supply connected to your AR-B9625 CPU board is turned off.

Step 4 : Connect all necessary cables. Make sure that the FDC, HDC, serial and parallel cables are connected to pin 1 of the related connector (not upside down).

Step 5 : Connect the hard disk/floppy disk flat cables from the CPU board to the drives. Connect a power source to each drive.

Step 6 : Plug the keyboard into the keyboard connector.

Step 7 : Turn on the power.

Step 8: Configure your system with the BIOS Setup program (section 6) then re-boot your system.

Step 9: If the CPU board does not work, turn off the power and read the hardware description carefully again.

Step 10: If the CPU board still does not perform properly, return the board to your dealer for immediate service.

5.2 UTILITY DISKETTE

The AR-B9625 provides two utility diskettes.

5.2.1 VGA and Audio Driver

The AR-B9625 provides video and audio function drivers for the WIN95 and WIN98, the driver can auto-setup in the WIN95 or WIN98 mode. The user must first decompress the compressed file.

Step 1: Extract the <WINCX_40.ZIP> file onto your hard drive, then generate the ZIP file into two files: the <License.pdf> is a Read Me document; and the <Cyrix MediaGX Certified Win9x Drivers 4.0.exe> is the function driver.

Step 2: In WIN95 or WIN98 mode execute the <Cyrix MediaGX Certified Win9x Drivers 4.0.exe> file, the system will auto-setup the video and audio functions.

5.2.2 Network Utility

There are two auto-extract files for the network utility. User must extract the files in DOS mode. Type in the full file name and press enter; the file will then self extract.

1. Autoextract the <ALL8139.EXE> file that includes the network drivers for various operating systems.

2. Autoextract the <SW8139.EXE> file that includes the testing and configuration files.

8139A.CFG	configuration file of the network
PG8139.EXE	LAN configuration EEPROM programmer
RSET8139.EXE	diagnostic and modification program

5.3 WATCHDOG TIMER

This section describes how to use the Watchdog Timer, disabled, enabled, and trigger.

The AR-B9625 is equipped with a programmable time-out period watchdog timer. You can use your own program to enable the watchdog timer. Once you have enabled the watchdog timer, the program should trigger the I/O every time before the timer times out. If your program fails to trigger or disable this timer before it times out, e.g. because of a system hang, the timer will generate a reset signal to reset the system. The time-out period can be programmed to be set from 3 to 42 seconds.

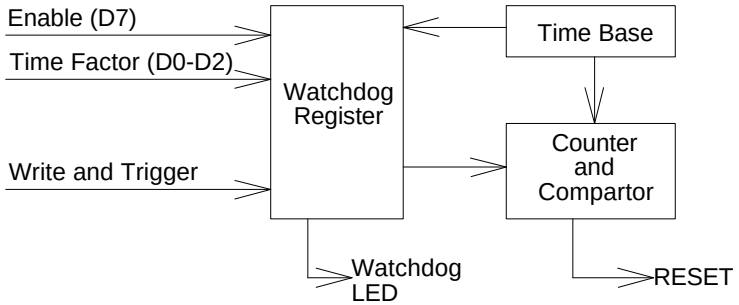


Figure 5-1 Watchdog Block Diagram

5.3.1 Watchdog Timer Setting

The watchdog timer is a circuit that may be used from your program software to detect crashes or hang-ups. Whenever the watchdog timer is enabled, the LED will blink to indicate that the timer is counting. The watchdog timer is automatically disabled after reset.

Once you have enabled the watchdog timer, your program must trigger the watchdog timer every time before it times-out. After you trigger the watchdog timer, it will be set to zero and start to count again. If your program fails to trigger the watchdog timer before time-out, it will generate a reset pulse to reset the system or trigger the IRQ15 signal to tell your program that the watchdog has timed out.

The factor of the watchdog timer time-out constant is approximately 6 seconds. The period for the watchdog timer time-out period is between 1 to 7 timer factors.

If you want to reset your system which decides when the watchdog times out, the following table lists the relation of timer factors between time-out period.

Time Factor	Time-Out Period (Seconds)
80H	3
81H	6
82H	12
83H	18
84H	24
85H	30
86H	36
87H	42

Table 5-1 Time-Out Setting

If you want to generate an IRQ15 signal to warn your program when the watchdog has timed out, the following table lists the relation of timer factors and time-out period.

Time Factor	Time-Out Period (Seconds)
0C0H	3
0C1H	6
0C2H	12
0C3H	18
0C4H	24
0C5H	30
0C6H	36
0C7H	42

Table 5-2 Time-Out Setting

NOTE: 1. If you program the watchdog to generate an IRQ15 signal when it times out, you should initial the IRQ15 interrupt vector and enable the second interrupt controller (8259 PIC) in order to enable CPU the to process this interrupt. An interrupt service routine is required too.
2. Before you initiate the interrupt vector of IRQ15 and enable the PIC, please enable the watchdog timer before hand, otherwise the watchdog timer will generate an interrupt at the time watchdog timer is enabled.

5.3.2 Watchdog Timer Enabled

To enable the watchdog timer, you have to output a byte of timer factor to the watchdog register whose address is 76H or Base Port+4. The following is a BASICA program which demonstrates how to enable the watchdog timer and set the time-out period at 24 seconds.

```
1000        REM Points to command register
1010              WD_REG% = 76H
1020        REM Timer factor = 84H (or 0C4H)
1030              TIMER_FACTOR% = %H84
1040        REM Output factor to watchdog register
1050              OUT WD_REG%, TIMER_FACTOR%
      .,etc.
```

5.3.3 Watchdog Timer Trigger

After you enable the watchdog timer, your program must write the same factor as enabling to the watchdog register at least once every time-out period to its previous setting. You can change the time-out period by writing another timer factor to the watchdog register at any time, and you must trigger the watchdog before the new time-out period in next trigger. Below is a BASICA program which demonstrates how to trigger the watchdog timer:

```
2000        REM Points to command register
2010              WD_REG% = 76H
2020        REM Timer factor = 84H (or 0C4H)
2030              TIMER_FACTOR% = &H84
2040        REM Output factor to watchdog register
2050              OUT WD_REG%, TIMER_FACTOR%
      .,etc.
```

5.3.4 Watchdog Timer Disabled

To disable the watchdog timer, simply write a 00H to the watchdog register.

```
3000        REM Points to command register
3010              WD_REG% = BASE_PORT% + 4
3020        REM Timer factor = 0
3030              TIMER_FACTOR% = 0
3040        REM Output factor to watchdog register
3050              OUT WD_REG%, TIMER_FACTOR%
      ., etc.
```

6. BIOS CONSOLE

This chapter describes the AR-B9625 BIOS menu displays and explains how to perform common tasks needed to get up and running, and presents detailed explanations of the elements found in each of the BIOS menus. The following topics are covered:

- BIOS Setup Overview
- Standard CMOS Setup
- Advanced CMOS Setup
- Advanced Chipset Setup
- Peripheral Setup
- Auto-Detect Hard Disks
- Password Setting
- Load Default Setting
- BIOS Exit

6.1 BIOS SETUP OVERVIEW

Once you enter Award BIOS CMOS Setup Utility by holding the "Delete" button during boot-up, the Main Menu will appear on the screen. The Main Menu allows you to select from various setup functions and two exit choices. Use arrow keys to select among the items and press <Enter> to accept or enter the sub-menu.

ROM PCI/ISA BIOS (2A434AVA)
CMOS SETUP UTILITY
AWARD SOFTWARE, INC.

STANDARD CMOS SETUP	INTEGRATED PERIPHERALS
BIOS FEATURES SETUP	SUPERVISOR PASSWORD
CHIPSET FEATURES SETUP	USER PASSWORD
POWER MANAGEMENT SETUP	IDE HDD AUTO DETECTION
PNP/PCI CONFIGURATION	SAVE & EXIT SETUP
LOAD BIOS DEFAULTS	EXIT WITHOUT SAVING
LOAD SETUP DEFAULTS	

Esc:	Quit	:	Select Item
F10:	Save & Exit Setup	(Shift) F2:	Change Color

Time, Date, Hard Disk Type …

Figure 6-1 BIOS: Setup Main Menu

CAUTION:
1. AR-B9625 BIOS the factory-default setting is used to the <LOAD BIOS DEFAULTS> Acrosser recommends using the BIOS default setting, unless you are very familiar with the setting function, or you can contact the technical support engineer.
2. If the BIOS settings are lost, the CMOS will detect the <LOAD SETUP DEFAULTS> to boot the operation system, this option will reduce the performance of the system. Acrosser recommends choosing the <LOAD BIOS DEFAULTS> in the main menu. This option gives best-case values that should optimize system performance.
3. The BIOS settings are described in detail in this section.

6.2 STANDARD CMOS SETUP

The <Standard CMOS Setup> option allows you to record some basic system hardware configuration and set the system clock and error handling. If the CPU board is already installed in a working system, you will not need to select this option anymore.

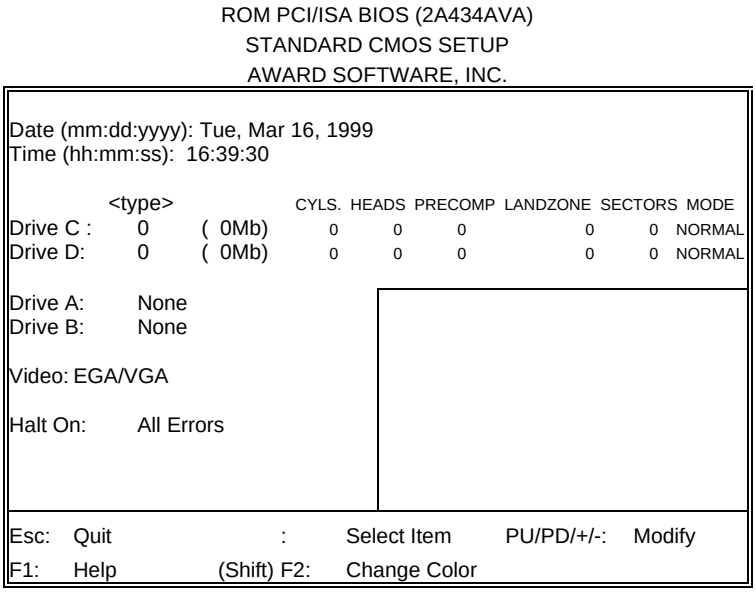


Figure 6-2 BIOS: Standard CMOS Setup

Date & Time Setup

Highlight the <Date> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the month, day and year format.
Highlight the <Time> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the hour, minute and second format.
The user can bypass the date and time prompts by creating an AUTOEXEC.BAT file. For information on how to create this file, please refer to the MS-DOS manual.

Hard Disk Setup

The BIOS supports various types for user settings, The BIOS supports <Pri Master>, <Pri Slave>, <Sec Master> and <Sec Slave> so the user can install up to two hard disks. For the master and slave jumpers, please refer to the hard disk' s installation descriptions and the hard disk jumper settings in section three of this manual.
You can select <AUTO> under the <TYPE> and <MODE> fields. This will enable auto detection of your IDE drives during boot-up. This will allow you to change your hard drives (with the power off) and then power on without having to reconfigure your hard drive type. If you use older hard disk drives which do not support this feature, then you must configure the hard disk drive in the standard method by choosing the HDD type, which should be noted directly on the HDD.

Floppy Setup

The <Standard CMOS Setup> option records the types of floppy disk drives installed in the system.
To enter the configuration value for a particular drive, highlight its corresponding field and then select the drive type using the left-or right-arrow key.

Video

This option selects the type of adapter used for the primary system monitor that must match your video display card and monitor. Although secondary monitors are supported, you do not have to select the type in Setup.

You have two ways to boot up the system:

1. When VGA as primary and monochrome as secondary, the selection of the video type is " VGA Mode".

2 When monochrome as primary and VGA as secondary, the selection of the video type is "Monochrome Mode".

.

EGA/VGA	Enhanced Graphics Adapter/Video Graphics Array. For EGA, VGA, SEGA, or PGA monitor adapters
CGA 40	Color Graphics Adapter, power up in 40 column mode
CGA 80	Color Graphics Adapter, power up in 80 column mode
MONO	Monochrome adapter, includes high resolution monochrome adapters

Error Halt

This option determines whether the computer will stop if an error is detected during power up.

No errors	The system boot will not be stopped for any error that may be detected.
All errors	Whenever the BIOS detects a non-fatal error the system will be stopped and you will be prompted.
All, But Keyboard	The system boot will not stop for a keyboard error, it will stop for all other errors.
All, But Diskette	The system boot will not stop for a disk error, it will stop for all other errors.
All, But Disk/Key	The system boot will not stop for a keyboard or disk error, it will stop for all other errors.

Memory

This option is display-only which is determined by POST (Power On Self Test) of the BIOS.

Base Memory

The POST of the BIOS will determine the amount of base (or conventional) memory installed in the system. The value of the base memory is typically 512K for systems with 512K memory installed on the motherboard, or 640K for systems with 640K or more memory installed on the motherboard.

Extended Memory

The BIOS determines how much extended memory is present during the POST. This is the amount of memory located above 1MB in the CPU's memory address map.

Other Memory

This refers to the memory located in the 640K to 1024K address space. This is memory that can be used for different applications. DOS uses this area to load device drivers to keep as much base memory free for application programs. Most use for this area is Shadow RAM.

Total Memory

System total memory is the sum of basic memory, extended memory, and other memory.

6.3 ADVANCED CMOS SETUP

The <Advanced CMOS SETUP> option consists of configuration entries that allow you to improve your system performance, or let you set up some system features according to your preference. Some entries here are required by the CPU board's design to remain in their default settings for optimal performance. It is suggested that you leave the settings on the factory default unless you are well versed in BIOS feaures.

ROM PCI/ISA BIOS (2A434AVA)
BIOS FEATURES SETUP
AWARD SOFTWARE, INC.

Virus Warning	: Enabled	Video BIOS Shadow	: Disabled
CPU Internal Cache	: Disabled	C8000-CBFFF Shadow	: Disabled
		CC000-CFFFF Shadow	: Disabled
Quick Power On Self Test	: Disabled	D0000-D3FFF Shadow	: Disabled
Boot Sequence	: A, C, SCSI	D4000-D7FFF Shadow	: Disabled
Swap Floppy Drive	: Disabled	D8000-DBFFF Shadow	: Disabled
Boot Up Floppy Seek	: Disabled	DC000-DFFFF Shadow	: Disabled
Boot Up NumLock Status	: Off		
Gate A20 Option	: Normal		
Memory Parity Check	: Disabled		
Typematic Rate Setting	: Disabled		
Typematic Rate (Chars/Sec)	: 6		
Typematic Delay (Msec)	: 250		
Security Option	: Setup		
PCI/VGA Palette Snoop	: Disabled	Esc: Quit	: Select Item
OS Select For DRAM > 64MB	: Non-OS2	F1: Help	PU/PD/+/-: Modify
Report No FDD For WIN 95	: No	F5: Old Values	(Shift) F2: Change Color
		F6: Load BIOS Defaults	
		F7: Load Setup Defaults	

Figure 6-3 BIOS: Advanced CMOS Setup

Virus Warning

This option may flash on the screen. During and after the system boots up, any attempt to write to the boot sector or partition table of the hard disk drive will halt the system and the following error message will appear, in the mean time, you can run an anti-virus program to locate the problem.

! WARNING !
Disk boot sector is to be modified
Type "Y" to accept write or "N" to abort write
Award Software, Inc.

The best remedy is to boot from the floppy drive and run a program to check for viruses. Then you may choose "Y" to accept.

Enabled	Activates automatically when the system boots up causing a warning message to appear when anything attempts to access the boot sector or hard disk partition table.
Disabled	No warning message to appear when anything attempts to access the boot sector or hard disk partition table. Windows 95/98 should choose this option.

Note: This function is available only for DOS and other OSes that do not trap INT13. This means that it can not be used on Windows 95/98.

CPU Internal Cache/External Cache

The two functions speed up memory access. However, it depends on CPU/chipset design. If your CPU is without Internal cache then this item <CPU Internal Cache> will not be show. The AR-B 9625's GXM Cyrix CPU has an internal cache and will automatically be set to <enabled>.

Quick Power On Self Test

This option speeds up Power On Self Test (POST) after you power on the computer. If it is set to Enable, BIOS will shorten or skip some items' checks during POST.

Boot Sequence
The option determines which drive computer searches first for the disk operating system.

Swap Floppy Drive
The option reverses the drive letter assignments of your floppy disk drives in the Swap A, B setting, otherwise leave on the default setting of ***Disabled*** (No Swap). This works separately from the BIOS Features floppy disk swap feature. It is functionally the same as physically interchanging the connectors of the floppy disk drives. When the function's setting is <***Enabled***>, the BIOS swapped floppy drive assignments so that Drive A becomes Drive B, and Drive B becomes Drive A under DOS.

Boot Up Floppy Seek
During POST, BIOS will determine if the floppy disk drive installed is 40 or 80 tracks. 360K type is 40 tracks while 760K, 1.2M and 1.44M are all 80 trackes.

Enabled	BIOS searches for floppy disk drive to determine if it is 40 or 80 tracks. Note that BIOS can not tell from 720K, 1.2M or 1.44M drive type as they are all 80 tracks.
Disabled	BIOS will not search for the type of floppy disk drive by track number. Note that there will not be any warning message if the drive installed is 360K.

Boot Up NumLock Status
This item is used to activate the NumLock function upon system boot. If the setting is on, after a boot, the NumLock light is lit, and the user can use the number keys.

Gate A20 Option
This item is chosen as <Normal>, the A20 signal is controlled by a keyboard controller or chipset hardware. The selection is "Fast" means the A20 signal is controlled by Port 92 or a chipset specific method.

Typematic Rate Setting
To enable typematic rate and typematic delay programming. If you disable the typematic rate and typematic delay programming, the system BIOS will use the default value of these 2 items and the default is controlled by the keyboard.

Typematic Rate (Chars/Sec)
Typematic Rate sets the rate at which characters on the screen repeat when a key is pressed and held down. The settings are 6, 8, 10, 12, 15, 20, 24, or 30 characters per second.

Typematic Delay (Msec)
The number selected indicates the time period between two identical characters appearing on screen.

Security Option
The option allows the user to limit access to the System and Setup, or just to Setup.

System	The system will not boot and access to Setup will de denied if the correct password is not entered at the prompt.
Setup	The system will boot, but access to Setup will be denied if the correct password is not entered at the prompt.

Note: To disable security, select PASSWORD SETTING at Main Menu and then you will be asked to enter password. Do not type anything and just press <Enter>, it will disable security. Once the security is disabled, the system will boot and you can enter Setup freely.

PCI/VGA Palette Snoop
This option must be set to Enabled if any ISA adapter card installed in the computer requires VGA palette snooping.

OS Select for DRAM > 64MB

This segment is specifically created for OS/2 when DRAM is larger than 64MB. If your operating system is OS/2 and DRAM used is larger the 64MB, you have to select <OS/2>, otherwise, non-OS2, default is NON-OS2.

Report No FDD for WIN95

If the user chooses "Yes" then Windows 95/98 searches. If "NO" then BIOS searches for the FDD.

Video BIOS Shadow

ROM Shadow copies Video BIOS code from slower ROM to faster RAM. Video BIOS can then execute from RAM. This makes your system faster.

C8000 – CFFFF Shadow/D8000 – DFFFF Shadow

The option determines whether optional ROM will be copied to RAM by 16K byte or 32K byte per/unit and the size depends on chipset. There are two blocks with 16K each. This may slow some systems with less memory.

Note:

1. For C8000-DFFFF option-ROM on PCI BIOS, BIOS will automatically enable the shadow RAM. User does not have to select the item.

2. IDE second channel control:
   Enable: Enable secondary IDE port and BIOS will assign IRQ15 for this port.
   Disable: Disable secondary IDE port and IRQ15 is available for other devices. The item is optional only for PCI BIOS.

3. Some of the sound cards have an onboard CD-ROM controller which uses IDE Secondary Port. In order to avoid PCI IDE conflict, the IDE secondary channel control has to select <Disable> then CD-ROM can work.

6.4 ADVANCED CHIPSET SETUP

This option controls the configuration of the board's chipset. Control keys for this screen are the same as for the previous screen. This selection is automatic.

ROM PCI/ISA BIOS (2A434AVA)
CHIPSET FEATURES SETUP
AWARD SOFTWARE, INC.

SDRAM CAS latency Time	: AUTO	
SDRAM Clock Ratio Div By	: 4	
16-bit I/O Recovery (CLK)	: 1	
8-bit I/O Recovery (CLK)	: 1	
		Esc: Quit : Select Item
		F1: Help PU/PD/+/-: Modify
		F5: Old Values (Shift) F2: Change Color
		F6: Load BIOS Defaults
		F7: Load Setup Defaults

Figure 6-4 BIOS: Advanced Chipset Setup

16-Bit I/O Cycle Recovery Time

8-Bit I/O Cycle Recovery Time

These options specify the length of the delay (in BUSCLK) inserted between consecutive 8-bit/16-bit I/O operations.

6.5 POWER MANAGEMENT

This section is designed to configure peripheral features.

ROM PCI/ISA BIOS (2A434AVA)
POWER MANAGEMENT SETUP
AWARD SOFTWARE, INC.

Power Management	: User Define	IRQ1	(KeyBoard)	: OFF
		IRQ3	(COM 2)	: OFF
** PM Timers **		IRQ4	(COM 1)	: OFF
Doze Mode	: Disabled	IRQ5	(LPT 2)	: OFF
Standby Mode	: Disabled	IRQ6	(Floppy Disk)	: OFF
HDD Power Down	: Disabled	IRQ7	(LPT 1)	: OFF
MODEM Use IRQ	: NA	IRQ9	(IRQ2 Redir)	: OFF
		IRQ10	(Reserved)	: OFF
Throttle Duty Cycle	: 12.5%	IRQ11	(Reserved)	: OFF
		IRQ12	(PS/2 Mouse)	: OFF
		IRQ13	(Coprocessor)	: OFF
		IRQ14	(Hard Disk)	: OFF
		IRQ15	(Reserved)	: OFF

Esc: Quit		:	Select Item
F1: Help	PU/PD/+/-:		Modify
F5: Old Values	(Shift) F2:		Change Color
F6: Load BIOS Defaults			
F7: Load Setup Defaults			

Figure 6-5 BIOS: Peripheral Setup

Power Management

The option determines how much power consumption is needed for the system after selecting the below items.

Doze Mode

Defines the continuous idle time before the system enters Doze Mode.

Standby Mode

Defines the continuous idle time before the system enters Standby Mode. If any item defined is enabled & active Standby timer will be reloaded.

HDD Power Down

This option specifies the power management states that the hard disk drive enters after the specified period of display inactivity has expired.

IRQ

These options enable event monitoring. When the computer is in a power saving mode, activity on the named interrupt request line is monitored by BIOS. When any activity occurs, the computer enters Full On mode.

6.6 INTEGRATED PERIPHERALS

This section is designed to configure the peripheral features.

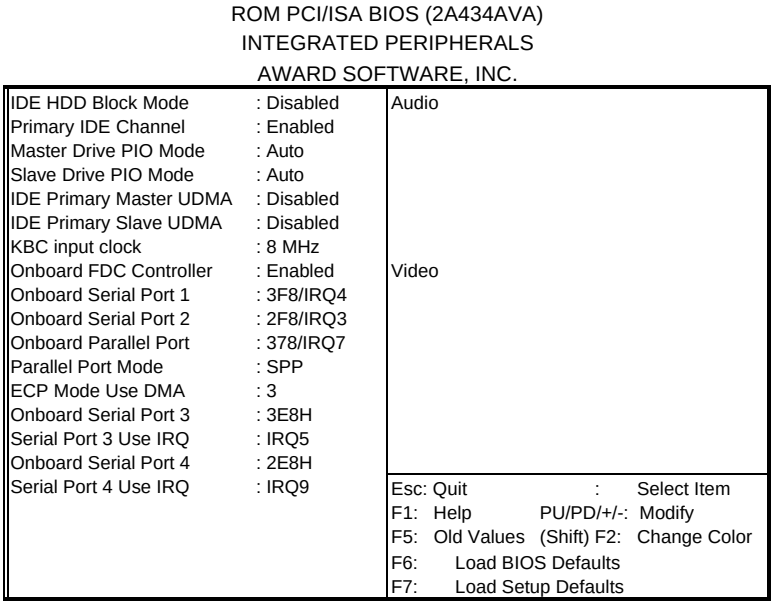


Figure 6-6 BIOS: Integrated Peripheral

IDE HDD Block Mode

This option allows your hard disk controller to use the fast block mode to transfer data to and from your hard disk drive (HDD).

Enabled	IDE controller uses block mode.
Disabled	IDE controller uses standard mode.

IDE PIO

IDE hard drive controllers can support up to two separate hard drives. These drives have a master/slave relationship which is determined by the cabling configuration used to attach them to the controller. Your system supports one IDE controller – a primary and a secondary – so you have the ability to install up to four separate hard disks.

PIO means Programmed Input/Output. Rather than have the BIOS issue a series of commands to effect a transfer to or from the disk drive, PIO allows the BIOS to tell the controller what it wants and then let the controller and the CPU perform the complete task by themselves. This is simpler and more efficient (and faster). Your system supports five modes, numbered from 0 to 4, which primarily differ in timing. When Auto is selected, the BIOS will select the best available mode.

OnBoard Parallel Port

This option is used to select the port address of the on-board parallel port. The options are 378H, 278H, 3BCH, and Disabled.

OnBoard Parallel Mode

This option specifies the parallel port Mode. The settings are Printer or Extended (Bi-direction).

OnBoard Serial Port

This option is used to select the port address of the on-board serial port A. The options are 3F8H, 2F8H, 3E8H, 2E8H, Auto and Disable. Port 1 is COM A, Port 2 is Com D and so on. Port four can be set to be IrDA (Choose Auto) if the IrDA device has been connected.

6.7 IDE HDD AUTO DETECTION

This option detects the parameters of an IDE hard disk drive, and automatically enters them into the Standard CMOS Setup screen.

6.8 PASSWORD SETTING

This BIOS Setup has an optional password feature. The system can be configured so that all users must enter a password every time the system boots or when BIOS Setup is executed.

6.8.1 Setting Password

Select the appropriate password icon from the Security section of the BIOS Setup main menu. Enter the password and press [Enter]. The screen does not display the characters entered. After the new password is entered, retype the new password as prompted and press [Enter].

If the password confirmation is incorrect, an error message appears. If the new password is entered without error, press [Esc] to return to the BIOS Main Menu. The password is stored in CMOS RAM after BIOS is completed. The next time the system boots, the prompt for the password function is present and is enabled.

```
Enter new supervisor password:
```

6.8.2 Password Checking

The password check option is enabled in Advanced Setup by choosing either ***Always*** (the password prompt appears every time the system is powered on) or ***Setup*** (the password prompt appears only when BIOS is run). The password is stored in CMOS RAM. User can enter a password by typing with the keyboard. Enter a 1-6 character password. The password does not appear on the screen when typed. Make sure you write it down.

6.9 LOAD DEFAULT SETTING

This section permits the user to select a group of settings for all BIOS Setup options. Not only can you use these items to quickly set system configuration parameters, you can choose a group of settings that have a better chance of working when the system is having configuration related problems.

6.9.1 Load BIOS Defaults

User can load the optimal default settings for the BIOS. The <LOAD BIOS DEFAULTS> uses best-case values that should optimize system performance. If CMOS RAM is corrupted, the optimal settings are loaded automatically.

```
Load high performance settings (Y/N) ?
```

6.9.2 Load Setup Defaults

User can load the <LOAD SETUP DEFAULTS> Setup option settings by selecting the Fail-Safe item from the Default section of the BIOS Setup main menu.
The Fail-Safe settings provide far from optimal system performance, but are the most stable settings. Use this option as a diagnostic aid if the system is behaving erratically.

```
Load failsafe settings (Y/N) ?
```

6.10 BIOS EXIT

This section is used to exit the BIOS main menu in two types of situation. After making your changes, you can either save them or exit the BIOS menu and without saving the new values.

6.10.1 Save & Exit Setup

This item set in the <Standard CMOS Setup>, <BIOS Features Setup>, <Chipset Features Setup>, <Power Management Setup>, <Integrated Peripherals> and the new password (if it has been changed) will be stored in the CMOS. The CMOS checksum is calculated and written into the CMOS.

As you select this function, the following message will appear at the center of the screen to assist you in saving data to CMOS and Exit the Setup.

```
Save current settings and exit (Y/N) ?
```

6.10.2 Exit Without Saving

When you select this option, the following message will appear at the center of the screen to help to Abandon all Data and Exit Setup.

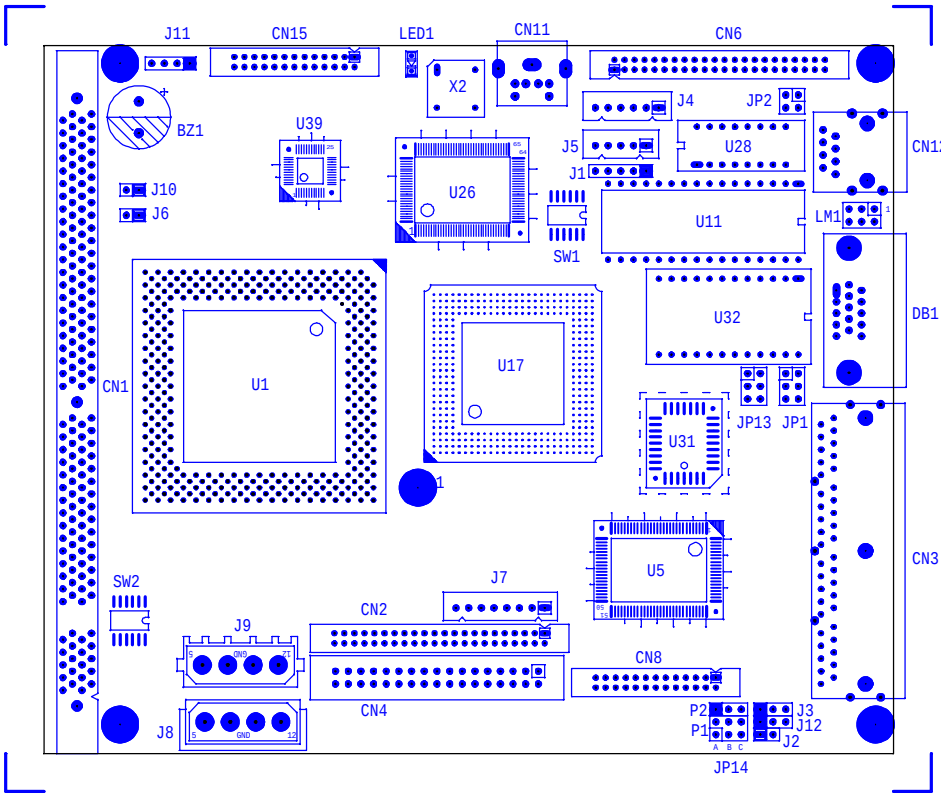
```
Quit without saving (Y/N) ?
```

7. SPECIFICATIONS

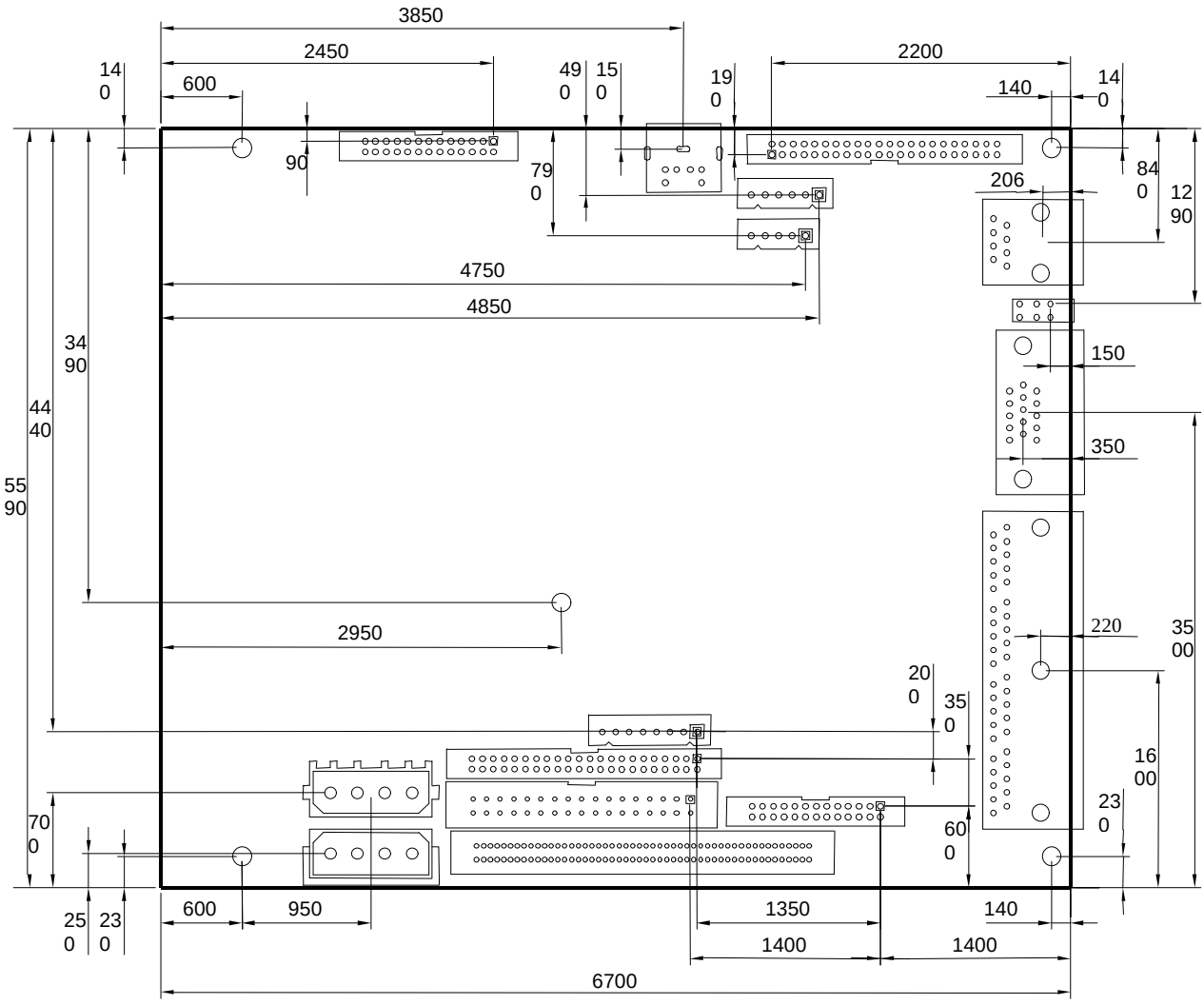
CPU:	Cyrix GXM-200 (or other GXM CPUs)
Chipset:	Cyrix CX5530
DRAM:	One 168-pin DIMM socket
Ethernet:	100/10-Base2, shielded RJ-45 edge connector
CRT/LCD Display:	Supports CRT (HDB-15 connector) and TFT-LCD
Audio:	16-bit PnP sound system
HDC:	Supports one PCI IDE that supports two hard disk drives
FDC:	Supports two 5.25" or 3.5" floppy disk drives
Serial Port:	4 full RS-232C port with phone-jack connector
Parallel Port:	1 bi-directional centronics type parallel port
Keyboard:	PC/AT compatible keyboard with 6-pin mini-din connector
PS/2 Mouse:	6-pin 2.5mm JST connector
Real Time Clock:	BQ3287MT or compatible chips
BIOS:	AWARD FLASH system BIOS
Watchdog:	Programmable watchdog timer
LED Indicator:	Power LED, LAN LED, HDD LED, and watchdog LED
Power Connector:	One 4-pin and one 8-pin (2.5mm) power connector
Power Req.:	+5V, 3A maximum, +12V, 0.5A maximum
PC Board:	6 layers
Dimensions:	146.1 mmX203.2mm (5.75"X8.00")

8. PLACEMENT & DIMENSIONS

8.1 PLACEMENT



8.2 DIMENSIONS



Unit: mil (1 inch = 25.4 mm = 1000 mil)

9. PROGRAMMING RS-485 & INDEX

9.1 PROGRAMMING RS-485

The majority of the communicative operations of the RS-485 are the same as the RS-232. When the RS-485 proceeds with transmission, which needs control the TXC signal (RS-232 and RS-485 control the signal differently), the installation steps are as follows:

Step 1: Enable TXC

Step 2: Send out data

Step 3: Waiting for data empty

Step 4: Disable TXC

NOTE: Please refer to the "Serial Port" section in the chapter "System Control" for the detailed description of the COM port's register.

(1) Initialize COM port

Step 1: Initialize COM port in the receiver interrupt mode, and /or transmitter interrupt mode. (All of the communication protocol buses of the RS-485 are the same.)

Step 2: Disable TXC (transmitter control), the bit 0 of the address of offset+4 just sets at "0".

NOTE: This is to control the AR-B9625 CPU card's DTR signal to the RS-485$ TXC communication.

(2) Send out one character (Transmit)

Step 1: Enable the TXC signal, and the bit 0 of the address of offset+4 just sets at "1".

Step 2: Send out the data. (Write this character to the offset+0 of the current COM port address)

Step 3: Wait for the buffer's data to empty. Check the transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) are all sets that must be at "0".

Step 4: Disabled the TXC signal, and the bit 0 of the address of offset+4 sets at "0"

(3) Send out one block data (Transmit – the data more than two characters)

Step 1: Enable the TXC signal, and the bit 0 of the address of offset+4 just sets at "1".

Step 2: Send out the data. (Write all data to the offset+0 of the current COM port address)

Step 3: Wait for the buffer's data to empty. Check the transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) are all sets thst must be at "0".

Step 4: Disabled the TXC signal, and the bit 0 of the address of offset+4 sets at "0".

(4) Receive data

The RS-485's operation of receiving data is the same as the RS-232's.

(5) Basic Language Example

a.) Initial 86C450 UART

```
10    OPEN “COM1:9600,m,8,1”AS #1 LEN=1
20    REM Reset DTR
30    OUT &H3FC, (INP(%H3FC) AND &HFA)
40    RETURN
```

b.) Send out one character to COM1

```
10    REM Enable transmitter by setting DTR ON
20    OUT &H3FC, (INP(&H3FC) OR &H01)
30    REM Send out one character
40    PRINT #1, OUTCHR$
50    REM Check transmitter holding register and shift register
60    IF ((INP(&H3FD) AND &H60) >0) THEN 60
70    REM Disable transmitter by resetting DTR
80    OUT &H3FC, (INP(&H3FC) AND &HEF)
90    RETURN
```

c.) Receive one character from COM1

```
10    REM Check COM1: receiver buffer
20    IF LOF(1)<256 THEN 70
30    REM Receiver buffer is empty
40    INPSTR$”
50    RETURN
60    REM Read one character from COM1: buffer
70    INPSTR$=INPUT$(1,#1)
80    RETURN
```

9.2 INDEX

Thank you for using the AR-B9625 user's manual!