

AR-B1542  
Half Size Pentium (586)  
CPU BOARD  
User' s Guide

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## 0.PREFACE

### 0.1 COPYRIGHT NOTICE AND DISCLAIMER

**September 1998**

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### 0.2 WELCOME TO THE AR-B1542 CPU BOARD

This guide introduces the Acrosser AR-B1542 CPU board.

The information provided in this manual describes this card's functions and features. It also helps you start, set up and operate your AR-B1542. General system information can also be found in this publication.

### 0.3 BEFORE YOU USE THIS GUIDE

Please refer to the Chapter 3, "Setting Up the System," in this guide, if you have not already installed this AR-B1542. Check the packing list before you install and make sure the accessories are completely included.

The AR-B1542 CD provides the newest information regarding the CPU card. **Please refer to the README.DOC file of the enclosed utility diskette.** It contains the modification, hardware & software information, it has updated to product functions that may not be mentioned here.

### 0.4 RETURNING YOUR BOARD FOR SERVICE

If your board requires any services, contact the distributor or sales representative from whom you purchased the product for service information. If you need to ship your board to us for service, be sure it is packed in a protective carton. We recommend that you keep the original shipping container for this purpose.

You can help assure efficient servicing for your product by following these guidelines:

1. Include your name, address, telephone, facsimile number and E-mail.
2. A description of the system configuration and/or software at the time is malfunction.
3. A brief description of problem occurred.

### 0.5 TECHNICAL SUPPORT AND USER COMMENTS

Users' comments are always welcome as they assist us in improving the quality of our products and the comprehension of our publications. They form a very important part of the input used for product enhancement and revision.

We may use and distribute any of the information you provide in any way appropriate without incurring any obligation. You may, of course, continue to use the information you supply.

If you have any suggestions for improving particular sections or if you find any errors on it, please send your comments to Acrosser Technology Co., Ltd. or your local sales representative and indicate the manual title and book number.

Internet electronic mail to: [webmaster@acrosser.com](mailto:webmaster@acrosser.com)

## 0.6 ORGANIZATION

This information for users covers the following topics (see the Table of Contents for a detailed listing):

- Chapter 1, "Overview", provides an overview of the system features and packing list.
- Chapter 2, "System Controller", describes the major structure.
- Chapter 3, "Setting Up the System", describes how to adjust the jumpers and the connector settings.
- Chapter 4, "Installation", describes setup procedures and information on the utility diskette.
- Chapter 5, "BIOS Console", provides the BIOS options settings.
- Chapter 6, Specifications
- Chapter 7, Placement & Dimensions
- Chapter 8, Programming RS-485 & Index

## 0.7 STATIC ELECTRICITY PRECAUTIONS

Before removing the board from its anti-static bag, read this section about static electricity precautions.

Static electricity is a constant danger to computer systems. The charge that can build up in your body may be more than sufficient to damage integrated circuits on any PC board. It is, therefore, important to observe basic precautions whenever you use or handle computer components. Although areas with humid climates are much less prone to static build-up, it is always best to safeguard against accidents may result in expensive repairs. The following measures should generally be sufficient to protect your equipment from static discharge:

- Touch a grounded metal object to discharge the static electricity in your body (or ideally, wear a grounded wrist strap).
- When unpacking and handling the board or other system component, place all materials on an antic static surface.
- Be careful not to touch the components on the board, especially the "golden finger" connectors on the bottom of every board.

# 1. OVERVIEW

This chapter provides an overview of your system features and capabilities. The following topics are covered:

- Introduction
- Packing List
- Features

## 1.1 INTRODUCTION

The AR-B1542 makes 333Hz, industrial computing a reality. Developed the small size and high speed systems, this half-size PCI card is excellent for embedded applications due to its stand alone operation.

Great speeds are attained through the PCI-driven IDE controllers. By providing a PCI interface to these two controllers, the AR-B1542 offers an exciting option for engineers involved in high performance projects. Also, the BIOS are available for the interface peripherals quickly and easily. The system's 4MB maximum shared memory for VGA display; 512KB synchronous pipeline burst SRAM, one RS-232C and one RS-232C/RS-485 serial port, and two 72-pin SIMM connectors that can support up to 128MB of DRAM.

The AR-B1542 is perfect for medical and telecommunications applications, factory floor networks, use as an MMI for high-speed processes, or a controller for graphics intensive systems.

## 1.2 PACKING LIST

The accessories are included with the system. Before you begin installing your AR-B1542 board, take a moment to make sure that the following items have been included inside the AR-B1542 package.

- The quick setup manual
- 1 AR-B1542 CPU board
- 1 Hard disk drive adapter cable
- 1 Floppy disk drive adapter cable
- 1 Parallel port adapter cable & 1 RS-232C interface cable mounted on one bracket
- 1 USB device adapter cable
- 4 Software utility CD

## 1.3 FEATURES

The system provides a number of special features that enhance its reliability, ensure its availability, and improve its expansion capabilities, as well as its hardware structure.

- Half size Pentium grade signal board computer
- Supports from 75MHz to 450MHz CPUs (ref. Section CPU Setting of Chapter 3)
- Up to 128MB DRAM system
- Up to 512KB PDSRAM L2 cache system
- On-board CRT display
- Supports IDE hard disk drives
- Supports floppy disk drives
- Supports 1 bi-directional parallel port
- Supports 2 serial ports (RS-232C and RS-485)
- PC/AT compatible keyboard and PS/2 mouse interface
- Programmable watchdog timer
- Flash BIOS
- Built-in status LEDs indicator
- Multi-layer PCB for noise reduction
- Dimensions: 122mmX185mm

## 2. SYSTEM CONTROLLER

This chapter describes the major structures of the AR-B1542 CPU board. The following topics are covered:

- DMA Controller
- Keyboard Controller
- Interrupt Controller
- Real-Time Clock and Non-Volatile RAM
- Serial Port
- Parallel Port

### 2.1 DMA CONTROLLER

The equivalent of two 8237A DMA controllers are implemented in the AR-B1542 board. Each controller is a four-channel DMA device that will generate the memory addresses and control signals necessary to transfer information directly between a peripheral device and memory. This allows high speed information transfer with less CPU intervention. The two DMA controllers are internally cascaded to provide four DMA channels for transferring to 8-bit peripherals (DMA1) and three channels for transferring to 16-bit peripherals (DMA2). DMA2 channel 0 provides the cascade interconnection between the two DMA devices, thereby maintaining IBM PC/AT compatibility.

The following is the system information of DMA channels:

DMA Controller 1	DMA Controller 2
Channel 0: Spare	Channel 4: Cascade for controller 1
Channel 1: IBM SDLC	Channel 5: Spare
Channel 2: Diskette adapter	Channel 6: Spare
Channel 3: Spare	Channel 7: Spare

Table 2-1 DMA Channel Controller

### 2.2 KEYBOARD CONTROLLER

The 8042 processor is programmed to support the keyboard serial interface. The keyboard controller receives serial data from the keyboard, checks its parity, translates scan codes, and presents it to the system as a byte data in its output buffer. The controller can interrupt the system when data is placed in its output buffer, or wait for the system to poll its status register to determine when data is available.

Data can be written to the keyboard by writing data to the output buffer of the keyboard controller.

Each byte of data is sent to the keyboard controller in series with an odd parity bit automatically inserted. The keyboard controller is required to acknowledge all data transmissions. Therefore, another byte of data will not be sent to keyboard controller until acknowledgment is received for the previous byte sent. The "output buffer full" interruption may be used for both send and receive routines.

### 2.3 INTERRUPT CONTROLLER

The equivalent of two 8259 Programmable Interrupt Controllers (PIC) are included on the AR-B1542 board. They accept requests from peripherals, resolve priorities on pending interrupts in service, issue interrupt requests to the CPU, and provide vectors which are used as acceptance indices by the CPU to determine which interrupt service routine to execute.

Following is the system information of interrupt levels:

Interrupt Level	Description
NMI	Parity check
CTRL1	CTRL2
IRQ 0	System timer interrupt from timer 8254
IRQ 1	Keyboard output buffer full
IRQ 2	
	IRQ8 : Real time clock
	IRQ9 : Rerouting to INT 0Ah from hardware IRQ2
	IRQ10 : USB (Ref. section Advanced Chipset Setup)
	IRQ11 : spare
	IRQ12 : spare (PS/2 mouse)
	IRQ13 : Math. coprocessor
	IRQ14 : Hard disk adapter
	IRQ15 : Reserved for watchdog
IRQ 3	Serial port 2
IRQ 4	Serial port 1
IRQ 5	Spare
IRQ 6	Floppy disk adapter
IRQ 7	Parallel port 1

Figure 2-1 Interrupt Controller

### 2.3.1 I/O Port Address Map

Hex Range	Device
000-01F	DMA controller 1
020-021	Interrupt controller 1
022-023	AR-B1542 : SiS 5598 Chipset Address
040-04F	Timer 1
050-05F	Timer 2
060-06F	8042 keyboard/controller
070-071	Real-time clock (RTC), non-maskable interrupt (NMI)
076-077	Watchdog
080-09F	DMA page registers
0A0-0A1	Interrupt controller 2
0C0-0DF	DMA controller 2
0F0	Clear Math Co-processor
0F1	Reset Math Co-processor
0F8-0FF	Math Co-processor
170-178	Fixed disk 1
1F0-1F8	Fixed disk 0
201	Game port
208-20A	EMS register 0
214-215	Watchdog
218-21A	EMS register 1
278-27F	Parallel printer port 3 (LPT 3)
2E8-2EF	Serial port 4 (COM 4)
2F8-2FF	Serial port 2 (COM 2)
300-31F	Prototype card/Streaming Type Adapter
378-37F	Parallel printer port 2 (LPT 2)
380-38F	SDLC, bisynchronous
3A0-3AF	Bisynchronous
3B0-3BF	Monochrome display and printer port 1 (LPT 1)
3C0-3CF	EGA/VGA adapter
3D0-3DF	Color/Graphics monitor adapter
3E8-3EF	Serial port 3 (COM 3)
3F0-3F7	Diskette controller
3F8-3FF	Serial port 1 (COM 1)

Table 2-2 I/O Port Address Map



### 2.3.2 PCI Bus Assignment (Bus1)

Pin	Signal Name	Pin	Signal Name
A1	NC	B1	-12V
A2	+12V	B2	NC
A3	NC	B3	GND
A4	NC	B4	NC
A5	+5V	B5	+5V
A6	-INTA	B6	+5V
A7	-INTC	B7	-INTB
A8	+5V	B8	-INTD
A9	PCICLK2	B9	-PREQ3
A10	+5V	B10	-PREQ1
A11	PCICLK3	B11	-PGND3
A12	GND	B12	GND
A13	GND	B13	GND
A14	-PGNT1	B14	PCICLK0
A15	-PCIRST	B15	GND
A16	+5V	B16	PCICLK1
A17	-PGNT0	B17	GND
A18	GND	B18	-PREQ0
A19	-PREQ2	B19	+5V
A20	AD30	B20	AD31
A21	NC	B21	AD29
A22	AD28	B22	GND
A23	AD26	B23	AD27
A24	GND	B24	AD25
A25	AD24	B25	NC
A26	-PGND2	B26	C/BE3
A27	NC	B27	AD23
A28	AD22	B28	GND
A29	AD20	B29	AD21
A30	GND	B30	AD19
A31	AD18	B31	NC
A32	AD16	B32	AD17
A33	NC	B33	C/BE2
A34	-FRAME	B34	GND
A35	GND	B35	-IRDY
A36	-TRDY	B36	NC
A37	GND	B37	-DEVSEL
A38	-STOP	B38	GND
A39	NC	B39	-PLOCK
A40	NC	B40	-PERR
A41	NC	B41	NC
A42	GND	B42	-SERR
A43	PAR	B43	NC
A44	AD15	B44	C/BE1
A45	NC	B45	AD14
A46	AD13	B46	GND
A47	AD11	B47	AD12
A48	GND	B48	AD10
A49	AD9	B49	GND

Table 2-3 PCI Bus Assignment

Pin	Signal Name	Pin	Signal Name
C1	C/BE0	D1	AD8
C2	NC	D2	AD7
C3	AD6	D3	NC
C4	AD4	D4	AD5
C5	GND	D5	AD3
C6	AD2	D6	GND
C7	AD0	D7	AD1
C8	+5V	D8	+5V
C9	-REQ64	D9	-ACK64
C10	+5V	D10	+5V
C11	+5V	D11	+5V

Table 2-4 PCI Bus Assignment

### 2.3.3 Real-Time Clock and Non-Volatile RAM

The AR-B1542 contains a real-time clock compartment that maintains the date and time in addition to storing configuration information about the computer system. It contains 14 bytes of clock, control registers and 114 bytes of general purpose RAM. Because of using CMOS technology, it consumes very little power and can be maintained for long period of time using an internal Lithium battery. The contents of each byte in the CMOS RAM are listed as follows:

Address	Description
00	Seconds
01	Second alarm
02	Minutes
03	Minute alarm
04	Hours
05	Hour alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Status register A
0B	Status register B
0C	Status register C
0D	Status register D
0E	Diagnostic status byte
0F	Shutdown status byte
10	Diskette drive type byte, drive A and B
11	Fixed disk type byte, drive C
12	Fixed disk type byte, drive D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2-byte CMOS checksum
30	Low actual expansion memory byte
31	High actual expansion memory byte
32	Date century byte
33	Information flags (set during power on)
34-7F	Reserved for system BIOS

Table 2-5 Real-Time Clock &amp; Non-Volatile RAM

### 2.3.4 Timer

The AR-B1542 provides three programmable timers, each with a timing frequency of 1.19 MHz.

Timer 0 The output of this timer is tied to interrupt request 0. (IRQ 0)

Timer 1 This timer is used to trigger memory refresh cycles.

Timer 2 This timer provides the speaker tone.  
Application programs can load different counts into this timer to generate various sound frequencies.

## 2.4 SERIAL PORT

The ACEs (Asynchronous Communication Elements ACE1 to ACE4) are not only used to convert parallel data to a serial format on the transmit side but also used to convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and half (five-bit format only) or two stop bits. The ACEs are capable of handling divisors of 1 to 65535, and produce a 16x clock for driving the internal transmitter logic.

Provisions are not only included the use of 16x clock to drive the receiver logic but also included the ACE as a completed MODEM control capability, and a processor interrupt system that may be software tailored to the computing time required handle the communications link.

The following table is summary of each ACE accessible register

DLAB	Port Address	Register
0	base + 0	Receiver buffer (read)
		Transmitter holding register (write)
0	base + 1	Interrupt enable
X	base + 2	Interrupt identification (read only)
X	base + 3	Line control
X	base + 4	MODEM control
X	base + 5	Line status
X	base + 6	MODEM status
X	base + 7	Scratched register
1	base + 0	Divisor latch (least significant byte)
1	base + 1	Divisor latch (most significant byte)

**Table 2-6 ACE Accessible Registers**

#### (1) Receiver Buffer Register (RBR)

Bit 0-7: Received data byte (Read Only)

#### (2) Transmitter Holding Register (THR)

Bit 0-7: Transmitter holding data byte (Write Only)

#### (3) Interrupt Enable Register (IER)

Bit 0: Enable Received Data Available Interrupt (ERBFI)  
 Bit 1: Enable Transmitter Holding Empty Interrupt (ETBEI)  
 Bit 2: Enable Receiver Line Status Interrupt (ELSI)  
 Bit 3: Enable MODEM Status Interrupt (EDSSI)  
 Bit 4: Must be 0  
 Bit 5: Must be 0  
 Bit 6: Must be 0  
 Bit 7: Must be 0

**(4) Interrupt Identification Register (IIR)**

- Bit 0: "0" if Interrupt Pending
- Bit 1: Interrupt ID Bit 0
- Bit 2: Interrupt ID Bit 1
- Bit 3: Must be 0
- Bit 4: Must be 0
- Bit 5: Must be 0
- Bit 6: Must be 0
- Bit 7: Must be 0

**(5) Line Control Register (LCR)**

- Bit 0: Word Length Select Bit 0 (WLS0)
- Bit 1: Word Length Select Bit 1 (WLS1)

WLS1	WLS0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

- Bit 2: Number of Stop Bit (STB)
- Bit 3: Parity Enable (PEN)
- Bit 4: Even Parity Select (EPS)
- Bit 5: Stick Parity
- Bit 6: Set Break
- Bit 7: Divisor Latch Access Bit (DLAB)

**(6) MODEM Control Register (MCR)**

- Bit 0: Data Terminal Ready (DTR)
- Bit 1: Request to Send (RTS)
- Bit 2: Out 1 (OUT 1)
- Bit 3: Out 2 (OUT 2)
- Bit 4: Loop
- Bit 5: Must be 0
- Bit 6: Must be 0
- Bit 7: Must be 0

**(7) Line Status Register (LSR)**

- Bit 0: Data Ready (DR)
- Bit 1: Overrun Error (OR)
- Bit 2: Parity Error (PE)
- Bit 3: Framing Error (FE)
- Bit 4: Break Interrupt (BI)
- Bit 5: Transmitter Holding Register Empty (THRE)
- Bit 6: Transmitter Shift Register Empty (TSRE)
- Bit 7: Must be 0

**(8) MODEM Status Register (MSR)**

- Bit 0: Delta Clear to Send (DCTS)
- Bit 1: Delta Data Set Ready (DDSR)
- Bit 2: Training Edge Ring Indicator (TERI)
- Bit 3: Delta Receive Line Signal Detect (DSLSD)
- Bit 4: Clear to Send (CTS)
- Bit 5: Data Set Ready (DSR)
- Bit 6: Ring Indicator (RI)
- Bit 7: Received Line Signal Detect (RSLD)

**(9) Divisor Latch (LS, MS)**

	<b>LS</b>	<b>MS</b>
Bit 0:	Bit 0	Bit 8
Bit 1:	Bit 1	Bit 9
Bit 2:	Bit 2	Bit 10
Bit 3:	Bit 3	Bit 11
Bit 4:	Bit 4	Bit 12
Bit 5:	Bit 5	Bit 13
Bit 6:	Bit 6	Bit 14
Bit 7:	Bit 7	Bit 15

<b>Desired Baud Rate</b>	<b>Divisor Used to Generate 16x Clock</b>
300	384
600	192
1200	96
1800	64
2400	48
3600	32
4800	24
9600	12
14400	8
19200	6
28800	4
38400	3
57600	2
115200	1

Table 2-7 Serial Port Divisor Latch

**2.5 PARALLEL PORT****(1) Register Address**

<b>Port Address</b>	<b>Read/Write</b>	<b>Register</b>
base + 0	Write	Output data
base + 0	Read	Input data
base + 1	Read	Printer status buffer
base + 2	Write	Printer control latch

Table 2-8 Registers' Address

**(2) Printer Interface Logic**

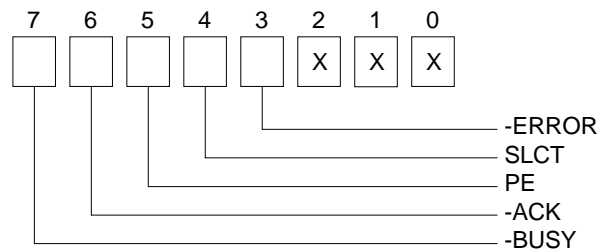
The parallel portion of the SMC37C669 makes the attachment of various devices that accept eight bits of parallel data at standard TTL level.

**(3) Data Swapper**

The system microprocessor can read the contents of the printer's Data Latch through the Data Swapper by reading the Data Swapper address.

**(4) Printer Status Buffer**

The system microprocessor can read the printer status by reading the address of the Printer Status Buffer. The bit definitions are described as follows:



**Figure 2-2 Printer Status Buffer**

**NOTE:** X presents not used.

**Bit 7:** This signal may become active during data entry, when the printer is off-line during printing, or when the print head is changing position or in an error state. When Bit 7 is active, the printer is busy and cannot accept data.

**Bit 6:** This bit represents the current state of the printer's ACK signal. A 0 means the printer has received the character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before receiving a BUSY message stops.

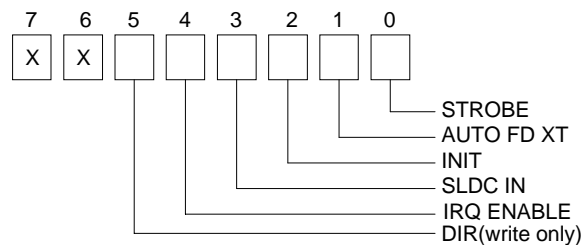
**Bit 5:** A 1 means the printer has detected the end of the paper.

**Bit 4:** A 1 means the printer is selected.

**Bit 3:** A 0 means the printer has encountered an error condition.

#### (5) Printer Control Latch & Printer Control Swapper

The system microprocessor can read the contents of the printer control latch by reading the address of printer control swapper. Bit definitions are as follows:



**Figure 2-3 Bit's Definition**

**NOTE:** X presents not used.

**Bit 5:** Direction control bit. When logic 1, the output buffers in the parallel port are disabled allowing data driven from external sources to be read; when logic 0, they work as a printer port. This bit is writing only.

**Bit 4:** A 1 in this position allows an interrupt to occur when ACK changes from low state to high state.

**Bit 3:** A 1 in this bit position selects the printer.

**Bit 2:** A 0 starts the printer (50 microseconds pulse, minimum).

**Bit 1:** A 1 causes the printer to line-feed after a line is printed.

**Bit 0:** A 0.5 microsecond minimum highly active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.

## 3. SETTING UP THE SYSTEM

This chapter describes pin assignments for the system's external connectors and jumpers setting.

- Overview
- System Setting
- How to Use the D.O.C.

### 3.1 OVERVIEW

The AR-B1542 is Pentium single CPU board. This section provides hardware's jumpers settings, connectors' locations, and the pin assignments.

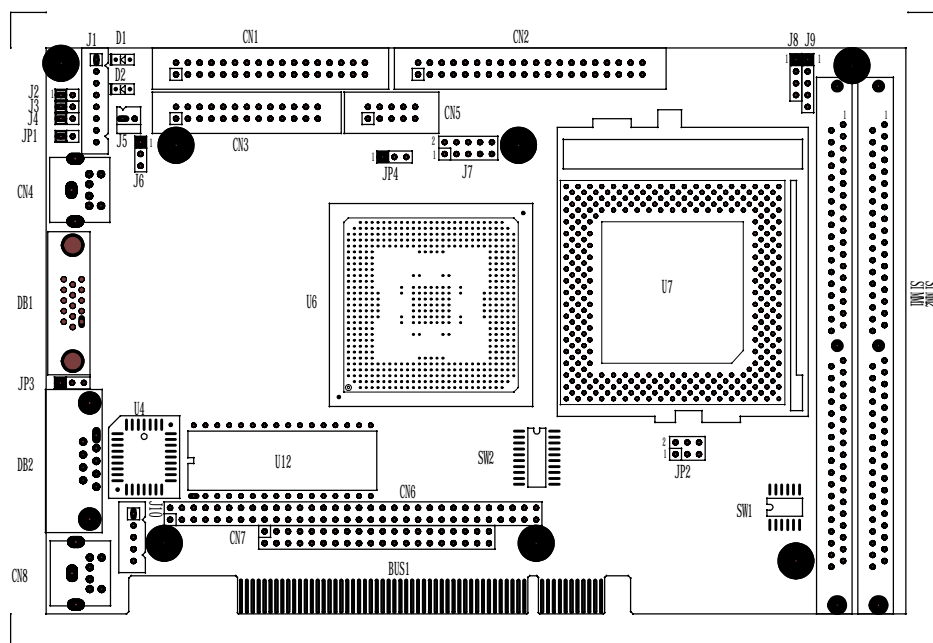


Figure 3-1 External System Location

### 3.2 SYSTEM SETTING

Jumper pins allow you to set specific system parameters. Set them by changing the pin location of jumper blocks. (A jumper block is a small plastic-encased conductor that slips over the pins.) To change a jumper setting, remove the jumper from its current location with your fingers or small needle-nosed pliers. Place the jumper over the two pins designated for the desired setting. Press the jumper evenly onto the pins. Be careful not to bend the pins.

We will show the locations of the AR-B1542 jumper pins, and the factory-default setting.

**CAUTION:** Do not touch any electronic component unless you are safely grounded. Wear a grounded wrist strap or touch an exposed metal part of the system unit chassis. The static discharges from your fingers can permanently damage electronic components.

### 3.2.1 PC/104 Connector

#### (1) 64-Pin PC/104 Connector Bus A & B (CN6)

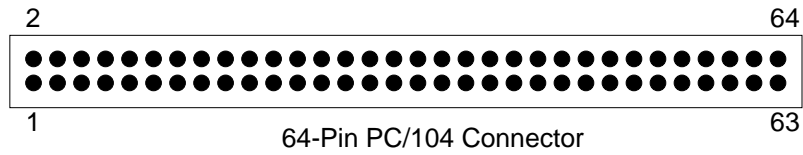


Figure 3-2 CN6: 64-Pin PC/104 Connector Bus A & B

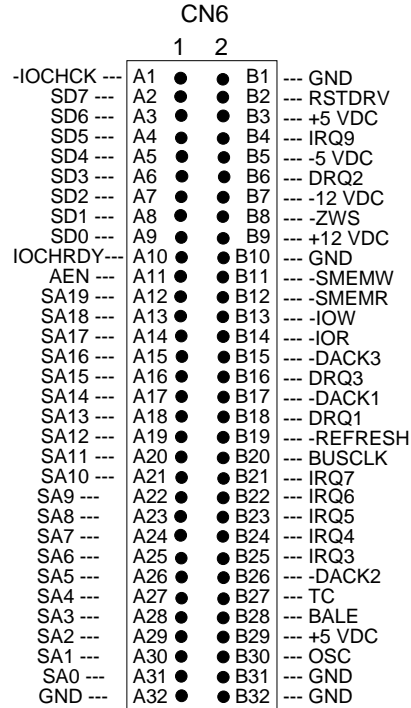


Figure 3-3 CN6: 64-Pin PC/104 Connector Bus A & B

#### (2) 40-Pin PC/104 Connector Bus C & D (CN7)

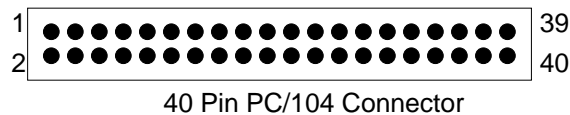


Figure 3-4 CN7: 40-Pin PC/104 Connector Bus C & D

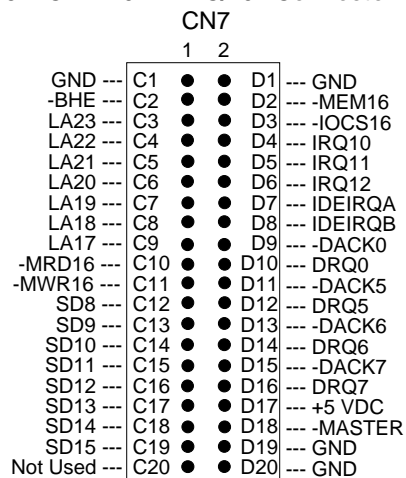


Figure 3-5 CN7: 40-Pin PC/104 Connector Bus C & D



**(3) PC/104 Bus Signal Description**

<b>Name</b>	<b>Description</b>
<b>BUSCLK</b> [Output]	The BUSCLK signal of the I/O channel is asynchronous to the CPU clock.
<b>RSTDRV</b> [Output]	This signal goes high during power-up, low line-voltage or hardware reset
<b>SA0 - SA19</b> [Input / Output]	The System Address lines run from bit 0 to 19. They are latched onto the falling edge of "BALE"
<b>LA17 - LA23</b> [Input/Output]	The Unlatched Address line run from bit 17 to 23
<b>SD0 - SD15</b> [Input/Output]	System Data bit 0 to 15
<b>BALE</b> [Output]	The Buffered Address Latch Enable is used to latch SA0 – SA19 onto the falling edge. This signal is forced high during DMA cycles
<b>-IOCHCK</b> [Input]	The I/O Channel Check is an active low signal which indicates that a parity error exist on the I/O board
<b>IOCHRDY</b> [Input, Open collector]	This signal lengthens the I/O, or memory read/write cycle, and should be held low with a valid address
<b>IRQ 3-7, 9-12, 14, 15</b> [Input]	The Interrupt Request signal indicates I/O service request attention. They are prioritized in the following sequence : (Highest) IRQ 9, 10, 11, 12, 13, 15, 3, 4, 5, 6, 7 (Lowest)
<b>-IOR</b> [Input/Output]	The I/O Read signal is an active low signal which instructs the I/O device to drive its data onto the data bus
<b>-IOW</b> [Input/Output]	The I/O write signal is an active low signal which instructs the I/O device to read data from the data bus
<b>-SMEMR</b> [Output]	The System Memory Read is low while any of the low 1mega bytes of memory are being used
<b>-MEMR</b> [Input/Output]	The Memory Read signal is low while any memory location is being read
<b>-SMEMW</b> [Output]	The System Memory Write is low while any of the low 1mega bytes of memory is being written
<b>-MEMW</b> [Input/Output]	The Memory Write signal is low while any memory location is being written
<b>DRQ 0-3, 5-7</b> [Input]	DMA Request channels 0 to 3 are for 8-bit data transfers. DMA Request channels 5 to 7 are for 16-bit data transfers. DMA request should be held high until the corresponding DMA has been completed. DMA request priority is in the following sequence:(Highest) DRQ 0, 1, 2, 3, 5, 6, 7 (Lowest)
<b>-DACK 0-3, 5-7</b> [Output]	The DMA Acknowledges 0 to 3, 5 to 7 are the corresponding acknowledge signals for DRQ 0 to 3 and 5 to 7
<b>AEN</b> [output]	The DMA Address Enable is high when the DMA controller is driving the address bus. It is low when the CPU is driving the address bus
<b>-REFRESH</b> [Input/Output]	This signal is used to indicate a memory refresh cycle and can be driven by the microprocessor on the I/O channel
<b>TC</b> [Output]	Terminal Count provides a pulse when the terminal count for any DMA channel is reached
<b>SBHE</b> [Input/Output]	The System Bus High Enable indicates the high byte SD8 - SD15 on the data bus

Name	Description
<b>-MASTER</b> [Input]	The MASTER is the signal from the I/O processor which gains control as the master and should be held low for a maximum of 15 microseconds or system memory may be lost due to the lack of refresh
<b>-MEMCS16</b> [Input, Open collector]	The Memory Chip Select 16 indicates that the present data transfer is a 1-wait state, 16-bit data memory operation
<b>-IOCS16</b> [Input, Open collector]	The I/O Chip Select 16 indicates that the present data transfer is a 1-wait state, 16-bit data I/O operation
<b>OSC</b> [Output]	The Oscillator is a 14.31818 MHz signal
<b>-ZWS</b> [Input, Open collector]	The Zero Wait State indicates to the microprocessor that the present bus cycle can be completed without inserting additional wait cycle

Table 3-1 PC/104 Bus Signal Description

### 3.2.2 Keyboard Connector

#### (1) 6-Pin Mini DIN Keyboard Connector (CN8)

CN8 is a Mini-DIN 6-pin connector. This keyboard connector is PS/2 type keyboard connector. This connector is also for a standard IBM-compatible keyboard that used the keyboard adapter cable.

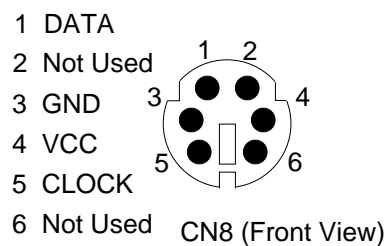


Figure 3-6 CN8: Keyboard Connector

#### (2) AUX. Keyboard Connector (J10)

A PC/AT compatible keyboard can be used by connected the provided adapter cable between J10 and the keyboard.

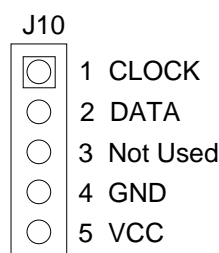


Figure 3-7 J10: AUX. Keyboard Connector

### 3.2.3 PS/2 Mouse Connector (CN4)

To use the PS/2 interface, an adapter cable has to be connected to the CN4 (6-pin header type) connector. The connector for the PS/2 mouse is a Mini-DIN 6-pin connector. Pin assignments for the PS/2 port connector are as follows:

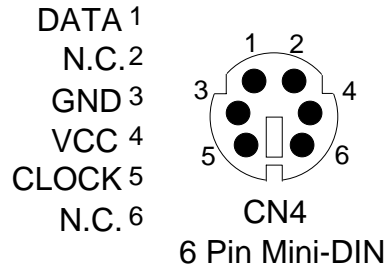


Figure 3-8 CN4: PS/2 Mouse Connector

### 3.2.4 Hard Disk (IDE) Connector (CN2)

A 40-pin header type connector (CN2) is provided to interface with up to two embedded hard disk drives (IDE AT bus). This interface, through a 40-pin cable, allows the user to connect up to two drives in a “daisy chain” fashion. To enable or disable the hard disk controller, please use the BIOS Setup program. The following table illustrates the pin assignments of the hard disk drive's 40-pin connector.

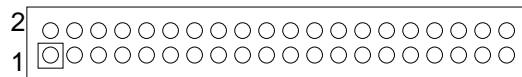


Figure 3-9 CN2: Hard Disk (IDE) Connector

Pin	Signal	Pin	Signal
1	-RESET	2	GROUND
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DATA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14
17	DATA 0	18	DATA 15
19	GROUND	20	NOT USED
21	DRQ A	22	GROUND
23	-IOW A	24	GROUND
25	-IOR A	26	GROUND
27	-CHRDY A	28	NOT USED
29	DACK A	30	GROUND
31	-IRQ A	32	NOT USED
33	SA 1	34	NOT USED
35	SA 0	36	SA 2
37	CS 0	38	CS 1
39	HD LED A	40	GROUND

Table 3-2 HDD Pin Assignment

### 3.2.5 FDD Port Connector (CN1)

The AR-B1542 provides a 34-pin header type connector for supporting up to two floppy disk drives. To enable or disable the floppy disk controller, please use the BIOS Setup program.

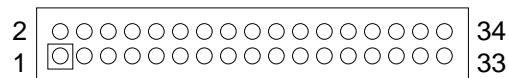


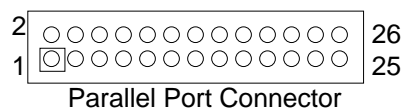
Figure 3-10 CN1: FDD Port connector

Pin	Signal	Pin	Signal
1-33(odd)	GROUND	18	DIRECTION
2	DRVEN 0	20	-STEP OUTPUT PULSE
4	NOT USED	22	-WRITE DATA
6	DRVEN 1	24	-WRITE ENABLE
8	-INDEX	26	-TRACK 0
10	-MOTOR ENABLE 0	28	-WRITE PROTECT
12	-DRIVE SELECT 1	30	-READ DATA
14	-DRIVE SELECT 0	32	-SIDE 1 SELECT
16	-MOTOR ENABLE 1	34	DISK CHANGE

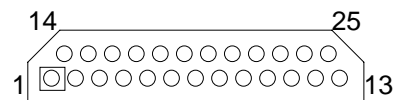
Table 3-3 FDD Pin Assignment

### 3.2.6 Parallel Port Connector (CN3)

To use the parallel port, an adapter cable has to be connected to the CN3 (26-pin header type) connector. The connector for the parallel port is a 25-pin D-type female connector.



Parallel Port Connector



DB-25

D-Type Connector

Figure 3-11 CN3: Parallel Port Connector

CN3	DB-25	Signal	CN3	DB-25	Signal
1	1	-Strobe	2	14	-Auto Form Feed
3	2	Data 0	4	15	-Error
5	3	Data 1	6	16	-Initialize
7	4	Data 2	8	17	-Printer Select In
9	5	Data 3	10	18	Ground
11	6	Data 4	12	19	Ground
13	7	Data 5	14	20	Ground
15	8	Data 6	16	21	Ground
17	9	Data 7	18	22	Ground
19	10	-Acknowledge	20	23	Ground
21	11	Busy	22	24	Ground
23	12	Paper	24	25	Ground
25	13	Printer Select	26	--	No Used

Table 3-4 Parallel Port Pin Assignments

### 3.2.7 Serial Port

#### (1) RS-232/RS-485 Select (JP3, JP4 & SW2-9)

JP4 selects COM B port, and adjusts the CN5 connector is RS-485 or RS-232C. JP3 selects COM A port for using DB2 for RS-232C or connects External RS-485. SW2-9 adjusts the onboard RS-485.

##### (A) COM-A RS-485 Adapter Select (JP3)

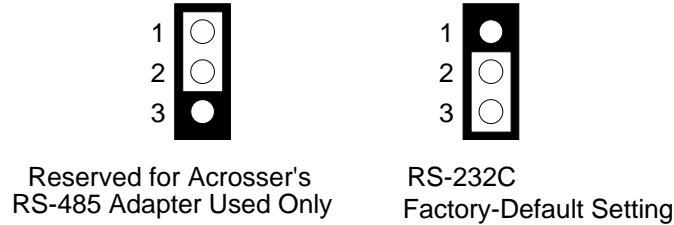


Figure 3-12 JP3: COM-A RS-485 Adapter Select

##### (B) COM-B RS-485 Adapter Select (JP4)

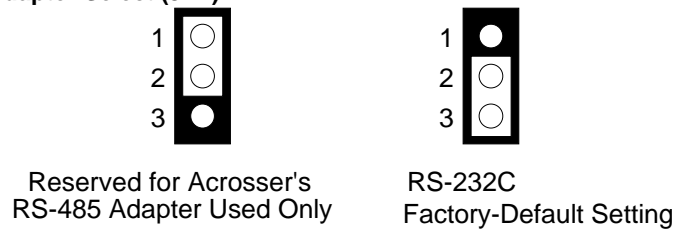


Figure 3-13 JP4: COM-B RS-485 Adapter Select

##### (C) COM-B RS-232C/RS-485 Select (SW2-9)

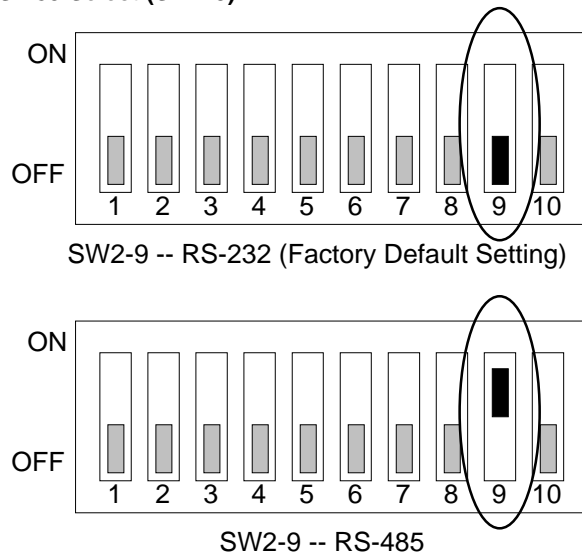


Figure 3-14 SW2-9: COM-B RS-232C/RS-485 Select

#### (2) RS-485 Terminator Select (JP1)

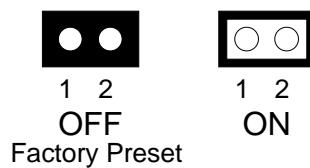
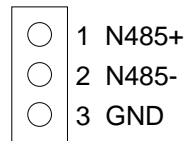


Figure 3-15 JP1: RS-485 Terminator Select

**(3) RS-485 Connector (J6)**

J6 is onboard RS-485 header. J6 pin assignments are as follows:

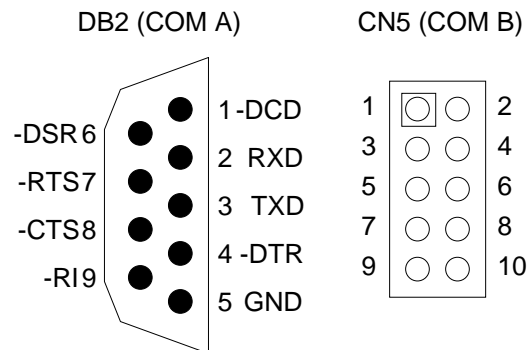


**J6 (COM B)**

**Figure 3-16 J6: RS-485 Connector**

**(4) RS-232 Connector (CN5 & DB2)**

There are two serial ports with EIA RS-232C interface on the AR-B1542. COM A uses one onboard D-type 9 pin male connector (DB2) and COM B uses one 10-pin header (CN5) which are located at the right side of the card. To configure these two serial ports, use the BIOS Setup program, and adjust the jumpers on JP3 and JP4. The pin assignments of the DB2 and CN5 for serial port A & B are as follows:



**Figure 3-17 DB2 & CN5: RS-232 Connector**

CN5	DB2	Signal	CN5	DB2	Signal
1	1	-DCD	2	6	-DSR
3	2	RXD	4	7	-RTS
5	3	TXD	6	8	-CTS
7	4	-DTR	8	9	-RI
9	5	GND	10	--	Not Used

**Table 3-5 Serial Port RS-232 Connector Pin Assignment**

### 3.2.8 USB Connector (J7)

USB is the abbreviation of Universal Serial Bus. The Universal Serial Bus (USB) standard is a low-to-medium speed interface for the connection of PC peripherals.

The USB standard simplifies the connection of peripherals to PCs with a uniform hardware and software interface. Personal computers equipped with USB allow computer peripherals to be automatically configured as soon as they are physically attached - without the need to reboot or run setup.

USB is a leading edge technology that allows the user to quickly and easily adding wide range peripheral devices from printers to keyboards and telephony devices to fax/modems. Universal Host Controller Interface (UHCI) and future support for the Open Host Controller Interface (OHCI) ensure USB compatibility and usability well into the future.

The connector on the CPU board supports two Universal Serial Bus ports. An optional external port bracket attaches to the onboard connector via an attached cable. With the optional port bracket installed you can attach USB devices to the external ports. If the USB ports are installed, the USB Controller line in the Integrated Peripherals section of the CMOS Setup utility must be set to "Enabled". USB ports may also require Operating System support for USB devices.

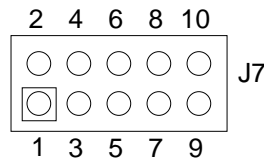


Figure 3-18 J7: USB Connector

Pin	Description	Pin	Description
1	VCC	2	VCC
3	-DATA	4	-DATA
5	+DATA	6	+DATA
7	GND	8	GND
9	CASE	10	CASE

Table 3-6 J7: USB Connector Pin Assignment

### 3.2.9 External Speaker Header (J8)

Besides the onboard buzzer, you can use an external speaker by connecting to the J8 header.

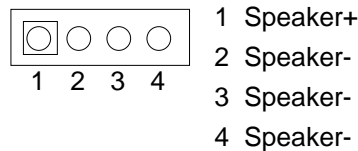


Figure 3-19 J8: External Speaker Header

### 3.2.10 Reset Header (J4)

J4 is used to connect to an external reset switch. Shorting these two pins will reset the system.

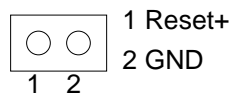


Figure 3-20 J4: Reset Header

### 3.2.11 LED Header

#### (1) External Power LED & Keyboard Lock Header (J9)

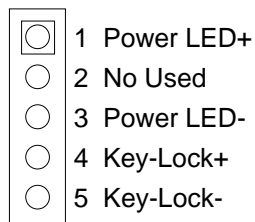


Figure 3-21 J9: Power LED & Keyboard Lock Header

#### (2) HDD LED Header (J3)

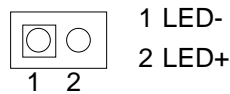


Figure 3-22 J3: HDD LED Header

#### (3) Watchdog LED Header (J2)

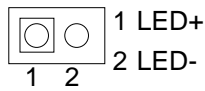


Figure 3-23 J2: Watchdog LED Header

### 3.2.12 Power Connector (J1)

J1 is an 8-pin power connector. You can directly connect the power supply to the onboard power connector for stand-alone applications.

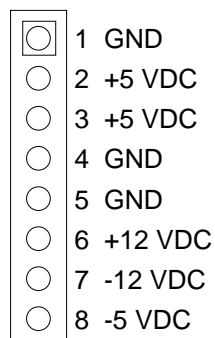


Figure 3-24 J1: 8-Pin Power Connector



### 3.2.13 CRT CONNECTOR (DB1)

The AR-B1542 supports CRT color monitors. AR-B1542 used onboard VGA chipset and user could adjust the VGA RAM in BIOS settings from 1MB to 4MB. For different VGA display modes, your monitor must possess certain characteristics to display the mode you want.

To connect to a CRT monitor, an adapter cable has to be connected to the DB1 connector. DB1 is used to connect with a VGA monitor when you are using the on-board VGA controller as a display adapter. Pin assignments for the DB1 connector are as follows:

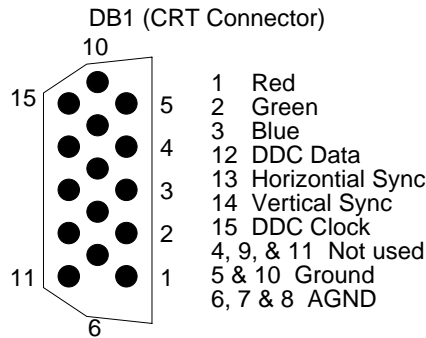


Figure 3-25 DB1: CRT Connector

### 3.2.14 CPU Setting

The AR-B1542 accepts many types of 586 microprocessors such as Intel Pentium, AMD K5 & AMD K6, Cyrix M1 and Cyrix M2. All of these CPUs include an integer processing unit, floating-point processing unit, memory-management unit, and cache. They can give a two to ten-fold performance improvement in speed over the 486 processor, which is depending on the clock speeds used and specific application. Like the 486 processor, the 586 processor includes both segment-based and page-based memory protection schemes. Instruction of processing time is reduced by on-chip instruction pipelining. By performing quickly, on-chip memory management and caching, the 586 processor relaxes requirements for memory response for a given level of system performance.

#### A. System Base Clock & CPU Clock Multiplier (SW2)



Figure 3-26 SW2: CPU Clock Multiplier

#### (1) CPU Base Clock Select (SW2)

This board supports different types of CPUs. The clock generator needs to be set by SW2. The CPU input clock is twice the operation clock.

SW2-4	SW2-5	SW2-6	Base Clock	PCI Clock
ON	ON	OFF	50MHz	25MHz
OFF	ON	OFF	66.6MHz	33.3MHz
ON	OFF	OFF	60MHz	30MHz
OFF	OFF	OFF	55MHz	27.5MHz
ON	ON	ON	51.3MHz	25.6MHz
OFF	ON	ON	68.4MHz	34.2MHz
ON	OFF	ON	61.6MHz	30.8MHz
OFF	OFF	ON	75MHz	37.5MHz

Table 3-7 SW2: CPU Clock Multiplier

**(2) CPU Clock Multiplier Select (SW2)**

The CPU clock multiplier needs to be set by SW2.

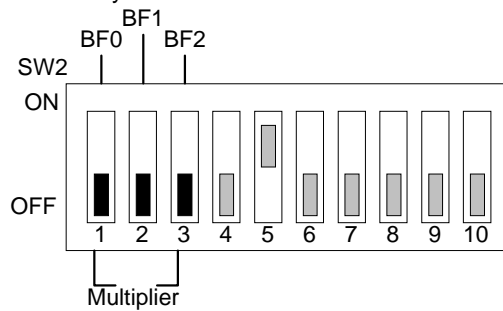
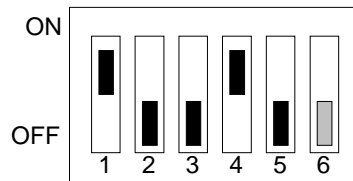


Figure 3-27 SW2: CPU Clock Multiplier

**B. CPU Logic Core Voltage Select (SW1)**

SW1 -- Factory Default Setting

Figure 3-28 SW1: CPU Logic Core Voltage

The following table lists the setup of CPU voltages from 1.96V to 3.46V.

SW1-1	SW1-2	SW1-3	SW1-4	SW1-5	SW1-6	Voltage
OFF	OFF	OFF	OFF	OFF	--	1.96V
ON	OFF	OFF	OFF	OFF	--	2.06V
OFF	ON	OFF	OFF	OFF	--	2.16V
ON	ON	OFF	OFF	OFF	--	2.2V
ON	ON	OFF	OFF	OFF	--	2.26V
OFF	OFF	ON	OFF	OFF	--	2.36V
ON	OFF	ON	OFF	OFF	--	2.4V
ON	OFF	ON	OFF	OFF	--	2.46V
OFF	ON	ON	OFF	OFF	--	2.56V
ON	ON	ON	OFF	OFF	--	2.66V
OFF	OFF	OFF	ON	OFF	--	2.76V
ON	OFF	OFF	ON	OFF	--	2.86V
OFF	ON	OFF	ON	OFF	--	2.96V
ON	ON	OFF	ON	OFF	--	3.06V
OFF	OFF	ON	ON	OFF	--	3.16V
ON	OFF	ON	ON	OFF	--	3.26V
OFF	ON	ON	ON	OFF	--	3.36V
ON	ON	ON	ON	OFF	--	3.46V

Table 3-8 SW1: CPU Logic Core Voltage

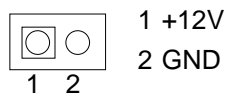
**C. CPU Cooling Fan Power Connector (J5)**

Figure 3-29 J5: CPU Cooling Fan Power Connector

D. P54C/P55C CPU Type Select (JP2)

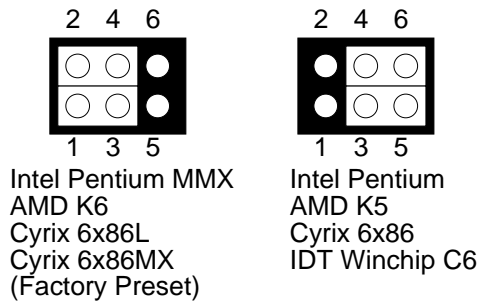


Figure 3-30 JP2: P55C/P54C CPU Type Select

Intel CPU

CPU Type	Work Frequency	SW2		SW2-1	SW2-2	SW2-3	SW1
		Clock	Multiplier	BF0	BF1	BF2	
Pentium - 75	75MHz	50.0MHz	1.5X	Off	Off	Off	3.36V
Pentium - 90	90MHz	60.0MHz	1.5X	Off	Off	Off	
Pentium - 100	100MHz	66.7MHz	1.5X	Off	Off	Off	
Pentium - 120	120MHz	60.0MHz	2.0X	On	Off	Off	
Pentium - 133	133MHz	66.7MHz	2.0X	On	Off	Off	
Pentium - 150	150MHz	60.0MHz	2.5X	On	On	Off	
Pentium - 166	166MHz	66.7MHz	2.5X	On	On	Off	
Pentium - 200	200MHz	66.7MHz	3.0X	Off	On	Off	
MMX-166	166MHz	66.7MHz	2.5X	On	On	Off	2.86V
MMX-200	200MHz	66.7MHz	3.0X	Off	On	Off	
MMX-233	233MHz	66.7MHz	3.5X	Off	Off	Off	

Table 3-9 Intel CPU Base Clock Setting

AMD CPU

CPU Type	Work Frequency	SW2		SW2-1	SW2-2	SW2-3	SW1
		Clock	Multiplier	BF0	BF1	BF2	
K5-PR75 (ABR)	75MHz	50.0MHz	1.5X	Off	Off	Off	3.46V
K5-PR90 (ABR)	90MHz	60.0MHz	1.5X	Off	Off	Off	
K5-PR100 (ABR)	100MHz	66.7MHz	1.5X	Off	Off	Off	
K5-PR120 (ABR)	90MHz	60.0MHz	1.5X	On	Off	Off	
K5-PR133 (ABR)	100MHz	66.7MHz	1.5X	On	Off	Off	
K5-PR166 (ABR)	116.7MHz	66.7MHz	1.75X	On	On	Off	
K5-PR75 (AFR)	75MHz	50.0MHz	1.5X	Off	Off	Off	3.36V
K5-PR90 (AFR)	90MHz	60.0MHz	1.5X	Off	Off	Off	
K5-PR100 (AFR)	100MHz	66.7MHz	1.5X	Off	Off	Off	
K5-PR120 (AFR)	90MHz	60.0MHz	1.5X	On	Off	Off	
K5-PR133 (AFR)	100MHz	66.7MHz	1.5X	On	Off	Off	
K5-PR166 (AFR)	116.7MHz	66.7MHz	1.75X	On	On	Off	
K6-166 (MMX)(ANR)	166MHz	66.7MHz	2.5X	On	On	Off	2.96V
K6-200 (MMX)(ANR)	200MHz	66.7MHz	3.0X	Off	On	Off	
K6-233 (MMX)(ANR)	233MHz	66.7MHz	3.5X	Off	Off	Off	3.36v
K6-2-300	300MHz	66.7MHz	4.5X	On	On	On	2.26V
K6-2-333	333MHz	66.7MHz	5.0X	Off	On	On	
K6-2-366	366MHz	66.7 MHz	5.5X	Off	Off	On	2.2V
K6-2-380	375MHz	75 MHz	5.0X	Off	On	On	
K6-2-400	400MHz	66.7MHz	6.0X	On	Off	Off	
K6-2-450	450MHz	75 MHz	6.0X	On	Off	Off	
K6-2-450	450MHz	75MHz	6.0X	On	Off	Off	2.4V
K6-3-400	400MHz	66.7MHz	6.0X	On	Off	Off	2.2V
K6-3-400	400MHz	66.7MHz	6.0X	On	Off	Off	2.4V
K6-3-450	450MHz	75 MHz	6.0X	On	Off	Off	

Table 3-10 AMD CPU Base Clock Setting

**Cyrix CPU**

CPU Type	Work Frequency	SW2		SW2-1	SW2-2	SW2-3	SW1
		Clock	Multiplier	BF0	BF1	BF2	
6X86-PR120	100MHz	50.0MHz	2.0X	On	Off	Off	3.36V
6X86-PR133	110MHz	55.0MHz	2.0X	On	Off	Off	
6X86-PR150	120MHz	60.0MHz	2.0X	On	Off	Off	
6X86-PR166	133MHz	66.7MHz	2.0X	On	Off	Off	
6X86-PR200	150MHz	75.0MHz	2.0X	On	Off	Off	
6X86L-PR120	100MHz	50.0MHz	2.0X	On	Off	Off	2.86V
6X86L-PR133	110MHz	55.0MHz	2.0X	On	Off	Off	
6X86L-PR150	120MHz	60.0MHz	2.0X	On	Off	Off	
6X86L-PR166	133MHz	66.7MHz	2.0X	On	Off	Off	
6X86L-PR200	150MHz	75.0MHz	2.0X	On	Off	Off	
6X86-PR166 (MMX)	150/133	60/66.7	2.5X/2X	On	On/Off	Off	2.96V
6X86-PR200 (MMX)	166/150	66.7/75	2.5X/2X	On	On/Off	Off	
6X86-PR233 (MMX)	200/188	66.7/75	3X/2.5X	Off/On	On	Off	
6X86-PR300 (MMX)	233MHz	66.7MHz	3.5X	Off	Off	Off	

Table 3-11 Cyrix CPU Base Clock Setting

**IDT Winchip CPU**

CPU Type	Work Frequency	SW2		SW2-1	SW2-2	SW2-3	SW1
		Clock	Multiplier	BF0	BF1	BF2	
IDT C6-180	180MHz	60.0MHz	3.0X	Off	On	Off	3.46V
IDT C6-200	200MHz	66.7MHz	3.0X	Off	On	Off	
IDT C6-225	225MHz	75.0MHz	3.0X	Off	On	Off	
IDT C6-240	240MHz	60.0MHz	4.0X	On	Off	On	

Table 3-12 IDT Winchip CPU Base Clock Setting

**NOTE:** Intel CPU Pentium MMX - 233 is factory default setting.

**3.2.15 DRAM Configuration**

There are two 32-bit memory banks on the AR-B1542 board. It can use one-side or double-side 256KX36 bit to 16MX36-bit SIMMs (Single-Line Memory Modules). This provides the user with up to 128MB of main memory. The 32-bit SIMM (without parity bit) also can be used on AR-B1542 board. There are seven on-board memory configurations available. Please refer to the following table for details:

SIMM2	SIMM1	Total Memory
256KX32(X36)	256KX32(X36)	2MB
512KX32(X36)	512KX32(X36)	4MB
1MX32(X36)	1MX32(X36)	8MB
2MX32(X36)	2MX32(X36)	16MB
4MX32(X36)	4MX32(X36)	32MB
8MX32(X36)	8MX32(X36)	64MB
16MX32(X36)	16MX32(X36)	128MB

Table 3-13 DRAMs' Configuration

**Caution:** it is suggested to use 2 SIMMs on board with the same brand, model, memory size and specification, so that the system can function normally.

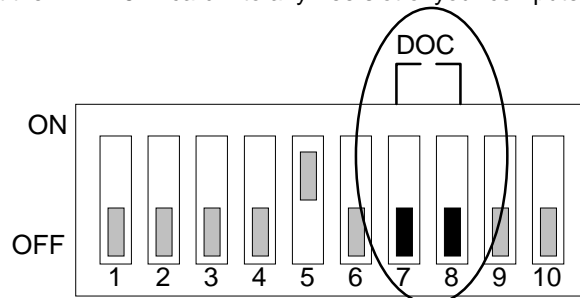
### 3.2.16 D.O.C. Memory Address Select (SW2-7 & SW2-8)

This section provides the information about how to use the D.O.C. (DiskOnChip). It is divided into two parts: hardware setting and software configuration.

**Step 1:** Use SW2 to select the correct D.O.C. memory address.

**Step 2:** Insert programmed DiskOnChip into sockets U19 setting as DOC.

**Step 3:** Line up and insert the AR-B1542 card into any free slot of your computer.



SW2 -- D.O.C. Memory Address  
(Factory Default Setting)

Figure 3-31 SW2-7 & SW2-8: D.O.C. Memory Address

SW2-7	SW2-8	Address	Note
OFF	OFF	CC00 : 0000	Factory Preset
OFF	ON	D000 : 0000	
ON	OFF	D400 : 0000	
ON	ON	D800 : 0000	

Table 3-14 D.O.C. Memory Address

## 4. INSTALLATION

This chapter describes the procedure of the utility diskette installation. The following topics are covered:

- Overview
- Utility Diskette
- Watchdog Timer

### 4.1 OVERVIEW

This chapter provides information for you to set up a working system based on the AR-B1542 CPU card. Please read the details of the CPU card's hardware descriptions before installation carefully, especially jumpers' setting, switch settings and cable connections.

Follow steps listed below for proper installation:

- Step 1 :** Read the CPU card's hardware description in this manual.
- Step 2 :** Install any DRAM SIMM onto the CPU card.
- Step 3 :** Set jumpers.
- Step 4 :** Make sure that the power supply connected to your passive backplane is turned off.
- Step 5 :** Plug the CPU card into a free PICMG slot on the backplane and secure it in place with a screw to the system chassis.
- Step 6 :** Connect all necessary cables. Make sure that the FDC, HDC, serial and parallel cables are connected to pin 1 of the related connector.
- Step 7 :** Connect the hard disk/floppy disk flat cables from the CPU card to the drives. Connect a power source to each drive.
- Step 8 :** Plug the keyboard into the keyboard connector.
- Step 9 :** Turn on the power.
- Step 10:** Configure your system with the BIOS Setup program then re-boot your system.
- Step 11:** If the CPU card does not work, turn off the power and read the hardware description carefully again.
- Step 12:** If the CPU card still does not perform properly, return the card to your dealer for immediate service.

### 4.2 UTILITY DISKETTE

AR-B1542 provides three VGA driver diskettes, supports WIN31, WIN95, WINNT3.5, WINNT 4.0 and OS/2 WARP 3.0.

There are three diskettes: disk 1 is for WIN31; disk2 is for WIN95 & IDE driver; disk 3 is for WINNT 3.5, WINNT 4.0 and OS/2. The utility disk attaches the README.DOC file, and after extracting the compressed files, including the README.TXT file in the decompressed sub-directories. Please refer to the README.TXT file for any troubleshooting before driver installation.

---

**CAUTION:** If you decompress files in the newly created directory, you can find the README file. It describes detailed installation information.

### 4.2.1 WIN 3.1 Driver

For the WIN31 operating system, the user must be in DOS mode to extract the compressed file. And then as to the steps:

- Step 1:** Make a new directory to contain the VGA drivers.  
C: \>MD VGAW31
- Step 2:** Insert the Utility Disk #1 in the floppy disk drive, and then copy the compressed file—WIN31DRV.EXE, and the file is self-extraction program. User can copy the file and execute the file in DOS mode.  
C: \>COPY A: \WI N31DRV. EXE C: \VGAW31
- Step 3:** Change directory to the newly created directory, and extract the compressed file. User can find that there are many files and one <windows> direction generated.  
  
C: \>CD VGAW31  
C: \VGAW31>WI N31DRV
- Step 4:** In WIN31 mode execute the SETUP.EXE file. It generates the SETUP MENU.  
C: \VGAW31>SETUP
- Step 5:** The screen shows SETUP TYPE window for choosing the three modes: <Typical>, <Compact>, <Custom>, and we can find the <Typical> mode is default setting. Please change the setting mode to <Custom>, it is necessary to choose the <Custom> mode, and click [next] button to enter the next setup step.
- Step 6:** Please only choose the <SVGA> item, the default setting is selected all items, so user has to change the selecting item, and then click [Next] button.
- Step 7:** Follow the setup steps' messages. As completed the setup procedure will generate the <Setup is complete> message and the <SiS Multimedia V1.07> program folder. And in the program folder user can find only one <uninstall> icon.
- Step 8:** In <Main Group> program folder, the <Windows setting> item we can find the <Display> item will appear <SiS 5597/5598 640x480 256 colors>, and other SiS 5597/5598 resolution, colors, font size, and so on. User can adjust the item for the VGA mode in WIN31.

### 4.2.2 WIN 95 Driver

For the WIN95 operating system, user must be in DOS mode to extract the compressed file, and then setup step by step:

- Step 1:** Make a new directory to contain the VGA drivers.  
C: \>MD VGAW95
- Step 2:** Insert the Utility Disk #2 in the floppy disk drive, and then copy the compressed file—WIN95DRV.EXE in the new directory.  
C: \>COPY A: \WI N95DRV. EXE C: \VGAW95
- Step 3:** Change directory to the newly created directory, and extract the compressed file.  
C: \>CD VGAW95  
C: \VGAW95>WI N95DRV
- Step 4:** Enter the WIN95 operating system and please choose the <SETTING> item of the <DISPLAY> icon in the {CONTROL PANEL}. Please select the <From Disk Install> item, and type the factory source files' path.  
C:\VGAW95
- Step 5:** Find the <SiS 5597/5598> item to select it and click the <OK> button.
- Step 6:** Finally, find the <SETTING> item in the <DISPLAY> icon. You can select this item, and adjust the <Screen Resolution>, <Font Size>...and other functions. Please refer to the messages during installation.

### 4.2.3 WINNT 4.0 Driver

For the WINNT4.0 operating system, the user must extract the compressed files in DOS mode. And then setup step by step:

- Step 1:** Make a new directory to contain the VGA drivers.  
C: \>MD VGANT40
- Step 2:** Insert the Utility Disk #3 in the floppy disk drive, and then copy the compressed file—NT40DRV.EXE in the new created directory.  
C: \>COPY A: \NT40DRV. EXE C: \VGANT40
- Step 3:** Change directory to the new directory, and extract the compressed file.  
C: \>CD VGANT40  
C: \VGANT40>NT40DRV
- Step 4:** Enter the WINNT4.0 operating system and choose the <SETTING> item of the <DISPLAY> icon in the {CONTROL PANEL}. Please select the <From Disk Install> item, and type the factory source files' path.  
C: \VGANT40
- Step 5:** Find the <SiS 5597/5598> item to select it and click the <OK> button.
- Step 6:** Find the <SETTING> item in the <DISPLAY> icon. You can select this item, and adjust the <Screen Resolution>, <Font Size>...and other function. Please refer to the messages during installation.

### 4.2.4 OS/2 Warp 3.0 Driver

The following steps must be performed before you install the SiS 5597/5598 display driver:

- 
- CAUTION:** 1. OS/2 DOS Support must be installed.  
2. If you previously installed SVGA support, you must do the following:  
a) Close all DOS Full Screen and WIN-OS2 sessions.  
b) Reset the system to VGA mode. VGA is the default video mode enabled when OS/2 is installed. To restore VGA mode, use Selective Install and select VGA for Primary Display. For more information on this procedure, see the section on Changing Display Adapter Support in the OS/2 Users Guide.

To install this driver, do the following steps:

- Step 1:** Open an OS/2 full screen or windowed session.
- Step 2:** Place the SiS 5597/5598 Display Driver Diskette in drive A. (DISK #3)
- Step 3:** Because the diskette enclosed a compressed file, extracted it with the following steps.
- Step 4:** In the OS/2-DOS mode, make a VGA directory for decompressing the driver.  
C: \>MD VGAOS2  
C: \>CD VGAOS2  
C: \VGAOS2>COPY A: \OS2DRV. EXE  
C: \VGAOS2>OS2DRV



- Step 5:** At the OS/2 command prompt, type the following commands to copy the files to the OS/2 drive:  
C:\VGAOS2> SETUP C:\VGAOS2 C: <ENTER>
- Step 6:** When the Setup Program is completed, you will need to perform a shutdown and then restart the system in order for changes to take effect.
- Step 7:** Please refer to the README.TXT file. When the installation is completed, adjust the VGA resolution in the SYSTEM icon <SCREEN> item of the <SYSTEM SETUP>.

### 4.3 WATCHDOG TIMER

This section describes how to use the Watchdog Timer, disabled, enabled, and trigger.

The AR-B1542 are equipped with a programmable time-out period watchdog timer. User can use the program to enable the watchdog timer. Once you have enabled the watchdog timer, the program should trigger it every time before it times out. If your program fails to trigger or disable this timer before it times out because of system hang, it will generate a reset signal to reset the system. The time-out period can be programmed to be 3 to 42 seconds.

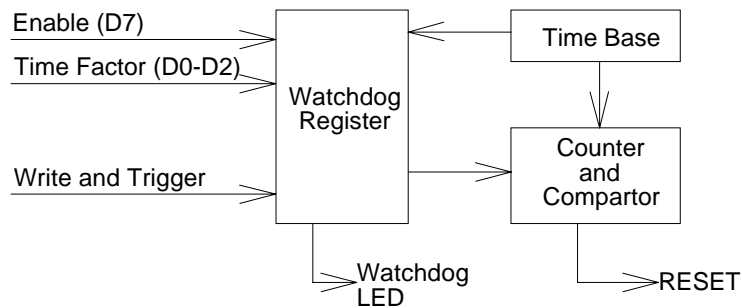


Figure 4-1 Watchdog Block Diagram

#### 4.3.1 Watchdog Timer Setting

The watchdog timer is a circuit that may be used from your program software to detect crashes or hang-ups. Whenever the watchdog timer is enabled, the LED will blink to indicate that the timer is counting. The watchdog timer is automatically disabled after reset.

Once you have enabled the watchdog timer, your program must trigger the watchdog timer every time before it times-out. After you trigger the watchdog timer, it will be set to zero and start to count again. If your program fails to trigger the watchdog timer before time-out, it will generate a reset pulse to reset the system or trigger the IRQ15 signal to tell your program that the watchdog is times out.

The factor of the watchdog timer time-out constant is approximately 6 seconds. The period for the watchdog timer time-out period is between 1 to 7 timer factors.

If you want to reset your system when watchdog times out, the following table listed the relation of timer factors between time-out periods.

Time Factor	Time-Out Period (Seconds)
80H	3
81H	6
82H	12
83H	18
84H	24
85H	30
86H	36
87H	42

Table 4-1 Time-Out Setting

If you want to generate IRQ15 signal to warn your program when watchdog times out, the following table lists the relation of timer factors and time-out period. And if you use the IRQ15 signal to warn your program when the watchdog times out, enter the BIOS Setup the <Peripheral Setup> menu, the <OnBoard PCI IDE> and <IDE Prefetch> items must set to **Primary**.

Time Factor	Time-Out Period (Seconds)
0C0H	3
0C1H	6
0C2H	12
0C3H	18
0C4H	24
0C5H	30
0C6H	36
0C7H	42

**Table 4-2 Time-Out Setting**

- NOTE:** 1. If you program the watchdog to generate IRQ15 signal when it times out, you should initial IRQ15 interrupt vector and enable the second interrupt controller (8259 PIC) in order to enable CPU to process this interrupt. An interrupt service routine is required too.
2. Before you initial the interrupt vector of IRQ15 and enable the PIC, please enable the watchdog timer previously, otherwise the watchdog timer will generate an interrupt at the time watchdog timer is enabled.

### 4.3.2 Watchdog Timer Enabled

To enable the watchdog timer, you have to output a byte of timer factor to the watchdog register whose address is 76H. The following is a BASICA program, which demonstrates how to enable the watchdog timer and set the time-out period at 24 seconds.

```

1000  REM Points to command register
1010      WD_REG% = 76H
1020  REM Timer factor = 84H (or 0C4H)
1030      TIMER_FACTOR% = %H84
1040  REM Output factor to watchdog register
1050      OUT WD_REG%, TIMER_FACTOR%
      .,etc.

```

### 4.3.3 Watchdog Timer Trigger

After you enable the watchdog timer, your program must write the same factor as enabling to the watchdog register at least once every time-out period to its previous setting. You can change the time-out period by writing another timer factor to the watchdog register at any time, and you must trigger the watchdog before the new time-out period in next trigger. Below is a BASICA program, which demonstrates how to trigger the watchdog timer:

```

2000  REM Points to command register
2010      WD_REG% = 76H
2020  REM Timer factor = 84H (or 0C4H)
2030      TIMER_FACTOR% = &H84
2040  REM Output factor to watchdog register
2050      OUT WD_REG%, TIMER_FACTOR%
      .,etc.

```

### 4.3.4 Watchdog Timer Disabled

To disable the watchdog timer, simply write a 00H to the watchdog register.

```

3000  REM Points to command register
3010      WD_REG% = 76H
3020  REM Timer factor = 0
3030      TIMER_FACTOR% = 0
3040  REM Output factor to watchdog register
3050      OUT WD_REG%, TIMER_FACTOR%
      ., etc.

```



## 5. BIOS CONSOLE

This chapter describes the BIOS menu displays and explains how to perform common tasks needed to get up and running. It also presents detailed explanations of the elements found in each of the BIOS menus. The following topics are covered:

- BIOS Setup Overview
- Standard CMOS Setup
- Advanced CMOS Setup
- Advanced Chipset Setup
- Power Management
- PCI/Plug and Play
- Peripheral Setup
- Auto-Detect Hard Disks
- Password Setting
- Load Default Setting
- BIOS Exit

### 5.1 BIOS SETUP OVERVIEW

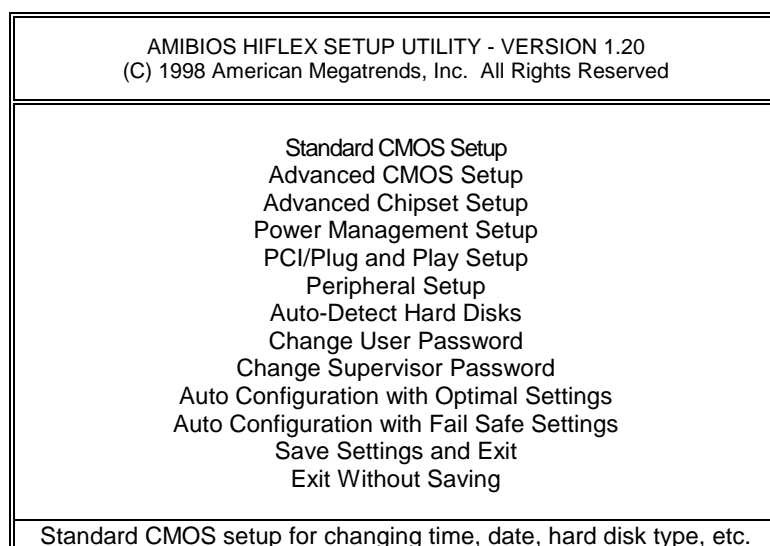
The BIOS is a program used to initialize and set up the I/O system of the computer, which includes the PCI bus and connected devices such as the video display, diskette drive, and the keyboard.

The BIOS provides a menu-based interface to the console subsystem. The console subsystem contains special software, called firmware that interacts directly with the hardware components and facilitates interaction between the system hardware and the operating system.

The BIOS default values ensure that the system will function at its normal capability. In the worst situation the user may have corrupted the original settings set by the manufacturer.

After the computer is turned on, the BIOS will perform diagnostics on the system and display the size of the memory that is being tested. Press the [Del] key to enter the BIOS Setup program, and then the main menu will show on the screen.

The BIOS Setup main menu includes some options. Use the [Up/Down] arrow key to highlight the option that you wish to modify, and then press the [Enter] key to select the option and configure the functions.



**Figure 5-1 BIOS: Setup Main Menu**

- CAUTION:** 1. In the AR-B1542 BIOS the factory-default setting is the <Auto Configuration with Optimal Settings>. Acrosser recommends using the BIOS default settings, unless you are very familiar with the setting function, or you can contact the technical support engineer.
2. If the BIOS loses setting, the CMOS will detect the <Auto Configuration with Fail Safe Settings> to boot the operating system. This option will reduce the performance of the system. Acrosser recommends choosing the <Auto Configuration with Optimal Setting> in the main menu. The option is best-case values that should optimize system performance.
3. The BIOS settings are described in detail in this section.

## 5.2 STANDARD CMOS SETUP

The <Standard CMOS Setup> option allows you to record some basic system hardware configurations and set the system clock and error handling. If the CPU board is already installed in a working system, you will not need to select this option anymore.

AMIBIOS SETUP - STANDARD CMOS SETUP									
(C) 1998 American Megatrends, Inc. All Rights Reserved									
Date (mm/dd/yyyy): Tue Jun 02, 1998					640KB				
Time (hh/mm/ss): 13:39:30					63MB				
Floppy Drive A:		1.44MB 3 ½							
Floppy Drive B:		Not Installed							
	Type	Size	Cyln	Head	Wpcom	Sec	LBA Mode	Blk Mode	PIO 32Bit Mode
Pri Master	: Auto						Off	Off	Auto Off
Pri Slave	: Auto						Off	Off	Auto Off
Boot Sector Virus Protection					Disabled				
Month: Jan - Dec					ESC:Exit ↑ ↓:Sel				
Day: 01 - 31					PgUp/PgDn:Modify				
Year: 1901 - 2099					F2/F3:Color				

**Figure 5-2 BIOS: Standard CMOS Setup**

### Date & Time Setup

Highlight the <Date> field and then press the [Page Up] / [Page Down] or [+]/[-] keys to set the current date. Follow the month, day and year format.

Highlight the <Time> field and then press the [Page Up] / [Page Down] or [+]/[-] keys to set the current date. Follow the hour, minute and second format.

The user can bypass the date and time prompts by creating an AUTOEXEC.BAT file. For information on how to create this file, please refer to the MS-DOS manual.

### Floppy Setup

The <Standard CMOS Setup> option records the types of floppy disk drives installed in the system.

To enter the configuration value for a particular drive, highlight its corresponding field and then select the drive type using the left-or right-arrow key.

## Hard Disk Setup

The BIOS supports various types for user settings, The BIOS supports <Pri Master> and <Pri Slave> so the user can install up to two hard disks. For the master and slave jumpers, please refer to the hard disk's installation descriptions and the hard disk jumper settings.

You can select <AUTO> under the <TYPE> and <MODE> fields. This will enable auto detection of your IDE drives during bootup. This will allow you to change your hard drives (with the power off) and then power on without having to reconfigure your hard drive type. If you use older hard disk drives, which do not support this feature, then you must configure the hard disk drive in the standard method as described above by the <USER> option.

## Boot Sector Virus Protection

This option protects the boot sector and partition table of your hard disk against accidental modifications. Any attempt to write to them will cause the system to halt and display a warning message. If this occurs, you can either allow the operation to continue or use a bootable virus-free floppy disk to reboot and investigate your system. The default setting is <Disabled>. This setting is recommended because it conflicts with new operating systems. Installation of new operating systems requires that you disable this to prevent write errors.

## 5.3 ADVANCED CMOS SETUP

The <Advanced CMOS Setup> option consists of configuration entries that allow you to improve your system performance, or let you set up some system features according to your preference. Some entries here are required by the CPU board's design to remain in their default settings.

AMBIOS SETUP - ADVANCED CMOS SETUP (C) 1998 American Megatrends, Inc. All Rights Reserved		
1st Boot Device	IDE-0	Available Options: Disabled IDE-0 IDE-1 IDE-2 IDE-3 Floppy ARMD-FDD ARMD-HDD CDROM SCSI NETWORK
2nd Boot Device	Floppy	
3rd Boot Device	CDROM	
4th Boot Device	Disabled	
Boot From Card BIOS	Yes	
Try Other Boot Devices	Yes	
S.M.A.R.T. for Hard Disks	Disabled	
Quick Boot	Disabled	
BootUp Num-Lock	On	
Floppy Drive Swap	Disabled	
Floppy Drive Seek	Disabled	
Floppy Access Control	Normal	
HDD Access Control	Normal	
PS/2 Mouse Support	Enabled	
Typematic Rate	Fast	
System Keyboard	Absent	
Primary Display	Absent	
Password Check	Setup	
Boot to OS/2, DRAM 64MB or Above	No	
Wait For 'F1' If Error	Disabled	
Hit 'DEL' Message Display	Enabled	
Internal Cache	WriteBack	
External Cache	WriteThru	
System BIOS Cacheable	Enabled	
C000, 16k Shadow	Enabled	
C400, 16k Shadow	Enabled	
C800, 16k Shadow	Disabled	
CC00, 16k Shadow	Disabled	
D000, 16k Shadow	Disabled	
D400, 16k Shadow	Disabled	
D800, 16k Shadow	Disabled	
DC00, 16k Shadow	Disabled	
		ESC:Exit ↑ ↓:Sel PgUp/PgDn:Modify F2/F3:Color

Figure 5-3 BIOS: Advanced CMOS Setup

### 1st Boot Device

### 2nd Boot Device

### 3rd Boot Device

### 4th Boot Device

These options determine where the system looks first for an operating system.

### Quick Boot

This category speeds up Power On Self Test (POST) after you power on the computer. If it is set to **Enabled**, BIOS will shorten or skip some check items during POST.

### BootUp Num-Lock

This item is used to activate the Num-Lock function upon system boot. If the setting is on, after a boot, the Num-Lock light is lit, and user can use the number key.

### Floppy Drive Swap

The option reverses the drive letter assignments of your floppy disk drives in the Swap A, B setting, otherwise leave on the setting of **Disabled** (No Swap). This works separately from the BIOS Features floppy disk swap feature. It is functionally the same as physically interchanging the connectors of the floppy disk drives. When **<Enabled>**, the BIOS swapped floppy drive assignments so that Drive A becomes Drive B, and Drive B becomes Drive A under DOS.

### Floppy Drive Seek

If the <Floppy Drive Seek> item is setting **Enabled**, the BIOS will seek the floppy <A> drive one time upon boot up.

### PS/2 Mouse Support

The setting of **Enabled** allows the system to detect a PS/2 mouse on boot up. If detected, IRQ12 will be used for the PS/2 mouse. IRQ 12 will be reserved for expansion cards if a PS/2 mouse is not detected. **Disabled** will reserve IRQ12 for expansion cards and therefore the PS/2 mouse will not function.

### Typematic Rate

This item specifies the speed at which a keyboard keystroke is repeated.

### System Keyboard

This function specifies that a keyboard would be attached to the computer.

### Primary Display

The option is used to set the type of video display card installed in the system.

### Password Check

This option enables password checking every time the computer is powered on or every time the BIOS Setup is executed. If **Always** is chosen, a user password prompt appears every time the computer is turned on. If **Setup** is chosen, the password prompt appears if the BIOS executed.

### Boot to OS/2, DRAM 64MB or Above

When using the OS/2 operating system with installed DRAM of greater than 64MB, you need to **Enabled** this option otherwise leave this on the setup default of **Disabled**.

**Wait for 'F1' If Error**

AMIBIOS POST error messages are followed by:

Press <F1> to continue

If this option is set to **Disabled**, the AMIBIOS does not wait for you to press the <F1> key after an error message.

**Hit 'DEL' Message Display**

Set this option to **Disabled** to prevent the message as follows:

Hit 'DEL' if you want to run setup

It will prevent the message from appearing on the first BIOS screen when the computer boots.

**Internal Cache**

This option specifies the caching algorithm used for L1 internal cache memory. The settings are:

Setting	Description
Disabled	Neither L1 internal cache memory on the CPU or L2 secondary cache memory is enabled.
WriteBack	Use the write-back caching algorithm.
WriteThru	Use the write-through caching algorithm.

**Table 5-1 Internal Cache Setting**

**External Cache**

This option specifies the caching algorithm used for L2 secondary (external) cache memory. The settings are:

Setting	Description
Disabled	Neither L1 internal cache memory on the CPU or L2 secondary cache memory is enabled.
WriteBack	Use the write-back caching algorithm.
WriteThru	Use the write-through caching algorithm.

**Table 5-2 External Cache Setting**

**System BIOS Cacheable**

When this option is set to **Enabled**, the contents of the F0000h system memory segment can be read from or written to L2 secondary cache memory. The contents of the F0000h memory segment are always copied from the BIOS ROM to system RAM for faster execution.

The settings are **Enabled** or **Disabled**. The <Optimal default settings> is **Enabled**. The <Fail-Safe default setting> is **Disabled**.



**Shadow**

These options control the location of the contents of the 32KB of ROM beginning at the specified memory location. If no adapter ROM is using the named ROM area, this area is made available to the local bus. The settings are:

<b>SETTING</b>	<b>DESCRIPTION</b>
Disabled	The video ROM is not copied to RAM. The contents of the video ROM cannot be read from or written to cache memory.
Enabled	The contents of C000h - C7FFFh are written to the same address in system memory (RAM) for faster execution.
Cached	The contents of the named ROM area are written to the same address in system memory (RAM) for faster execution, if an adapter ROM will be using the named ROM area. Also, the contents of the RAM area can be read from and written to cache memory.

**Table 5-3 Shadow Setting**

## 5.4 ADVANCED CHIPSET SETUP

This option controls the configuration of the board's chipset. Control keys for this screen are the same as for the previous screen.

AMIBIOS SETUP - ADVANCED CHIPSET SETUP (C) 1998 American Megatrends, Inc. All Rights Reserved		
DRAM Automatic Configuration	Enabled	Available Options : Disabled Enabled
EDO Dram Access Time	60ns	
FP Dram Access Time	None Used	
Refresh Cycle Time	187.2US	
RAS Pulse Width When Refresh	7T	
DRAM Read Leadoff Time	1T	
ISA Bus Clock Frequency	7.159MHZ	
MEMORY HOLE at 15M - 16M	Disabled	
USB Function	Disabled	
USB Keyboard / Mouse Legacy Support	Disabled	
VGA Shared Memory Size	1M	ESC:Exit ↑ ↓ :Sel
VGA Frequency	55MHz	PgUp/PgDn:Modify F2/F3:Color

Figure 5-4 BIOS: Advanced Chipset Setup

### DRAM Automatic Configuration

If selecting a certain setting for one BIOS Setup option determines the settings for one or more other BIOS Setup options, the BIOS automatically assigns the dependent settings and does not permit the end user to modify these settings unless the setting for the parent option is changed. Invalid options are grayed and cannot be selected.

### Memory Hole at 15-16 MB

This option specifies the range 15MB to 16MB in memory that cannot be addressed on the ISA bus.

### ISA Bus Clock Frequency

This option is used to select the ISA bus clock rate.

### USB Function

### USB Keyboard/Mouse Legacy Support

These options are used to <Enabled> the USB function and it is only useful in the DOS mode. The USB function sets <Enabled> will occupy IRQ10.

### VGA Shared Memory Size

This option sets the VGA's occupied memory size.

### VGA Frequency

This option sets the display's refresh.

### AT Bus Clock

This option sets the polling clock speed of ISA Bus (PC/104).

- 
- NOTE:** 1. PCLK means the CPU inputs clock.  
2. Acrosser recommends user setting at the range of 8MHz to 10MHz.

### Slow Refresh

This option sets the DRAM refresh cycle time.

**RAS Precharge Time**

The DRAM RAS precharge time.

**Time Insert Wait**

The DRAM time insert wait: RAS Active and CAS Precharge function setting.

**ISA High Speed**

The Speed field shows the speed at which the processor runs internally.

**I/O Recovery**

If I/O Recovery Feature options are enabled, the BIOS insert a delay time between two I/O commands. The delay time is defined in I/O Recovery Period option.

**5.5 POWER MANAGEMENT**

This section is used to configure power management features. This <Power management Setup> option allows you to reduce power consumption. This feature turns off the video display and shuts down the hard disk after a period of inactivity.

AMIBIOS SETUP - Power Management Setup (C) 1998 American Megatrends, Inc. All Rights Reserved		
Power Management /APM	Enabled	Available Options : Disabled Enabled
Video Power Down Mode	Disabled	
Hard Disk Power Down Mode	Disabled	
Hard Disk Time Out (Minute)	Disabled	
Standby Time Out (Minute)	Disabled	ESC:Exit ↑ ↓:Sel PgUp/PgDn:Modify F2/F3:Color
Suspend Time Out (Minute)	Disabled	
Slow Clock Ratio	1:4	
IRQ 3 – (COM2, COM4)	Monitor	
IRQ 4 – (COM1, COM3)	Monitor	
IRQ 5 – (LPT 2)	Ignore	
IRQ 7 – (LPT 1)	Monitor	
IRQ 9	Ignore	
IRQ 10	Ignore	
IRQ 11	Ignore	
IRQ 12 (PS2 Mouse)	Monitor	
IRQ 14	Monitor	
IRQ 15	Monitor	

**Figure 5-5 BIOS: Power Management Setup**

**Power Management /APM**

**Enabled** this option is to enable the power management and APM (Advanced Power Management) features.

**Video Power Down Mode**

This option specifies the power management states that the video subsystem enters after the specified period of display inactivity have expired.

**Hard Disk Power Down Mode**

This option specifies the power management states that the hard disk drive enters after the specified period of display inactivity have expired.

**Hard Disk Time Out**

This option specifies the length of a period of hard disk inactivity. When this period expired, the hard disk drive enters the power-conserving mode specified on the <Hard Disk Power Down Mode> option.

**Standby Time Out**

### Suspend Time Out

These options specify the length of the period of system inactivity when the computer is already in Standby mode before the computer is placed on Suspend mode. In Suspend mode, nearly all power use is curtailed.

### Slow Clock Ratio

This option specifies the speed at which the system clock runs in power saving modes. The settings are expressed as a ratio between the normal clock speed and the power down clock speed.

### IRQ

These options enable event monitoring. When the computer is in a power saving mode, activity on the named interrupt request line is monitored by BIOS. When any activity occurs, the computer enters Full On mode.

## 5.6 PCI/PLUG AND PLAY

This section is used to configure PCI / Plug and Play features. The <PCI & PNP Setup> option configures the PCI bus slots. All PCI bus slots on the system use INTA#, thus all installed PCI cards must be set to this value.

AMIBIOS SETUP - PCI/PLUG AND PLAY SETUP (C) 1998 American Megatrends, Inc. All Rights Reserved		
Plug and Play Aware O/S	Yes	Available Options : Yes No
Clear NVRAM	No	
PCI Latency Timer (PCI Clocks)	64	
PCI IDE BusMaster	Disabled	
DMA Channel 0	PnP	
DMA Channel 1	PnP	
DMA Channel 3	PnP	
DMA Channel 5	PnP	
DMA Channel 6	PnP	
DMA Channel 7	PnP	
IRQ 3	PCI /PnP	
IRQ 4	PCI /PnP	
IRQ 5	PCI /PnP	
IRQ 7	PCI /PnP	
IRQ 9	PCI /PnP	
IRQ 10	PCI /PnP	
IRQ 11	PCI /PnP	
IRQ 12	PCI /PnP	
IRQ 14	PCI /PnP	
IRQ 15	PCI /PnP	
Reserved Memory Size	Disabled	ESC:Exit ↑ ↓:Sel
Reserved Memory Address	C800	PgUp/PgDn:Modify F2/F3:Color

Figure 5-6 BIOS: PCI / Plug and Play Setup

### Plug and Play Aware O/S

Set this option to **Yes** if the operating system installed in the computer is Plug and Play-aware. The BIOS only detects and enables PnP ISA adapter cards that are required for system boot. The Windows 95 operating system detects and enables all other PnP-aware adapter cards. Windows 95 is PnP-aware. Set this option **<No>** if the operating system (such as DOS, OS/2, Windows 3.x) does not use PnP. You must set this option correctly or PnP-aware adapter cards installed in your computer will not be configured properly.

### Clear NVRAM

This sets the operating mode of the boot block area of the BIOS FLASH ROM to allow programming in the **Yes** setting.

### PCI Latency Timer (PCI Clocks)

This option sets latency of all PCI devices on the PCI bus. The settings are in units equal to PCI clocks.

### PCI IDE Bus Master

**Enabled** this option is to specify that the IDE controller on the PCI local bus has bus mastering capability.

**DMA & IRQ**

These options specify the bus that the named IRQs/DMA lines are used on. These options allow you to specify IRQs/DMA for use by legacy ISA adapter cards. These options determine if the BIOS should remove an IRQ/DMA from the pool of available IRQs/DMA passed to BIOS configurable devices. If more IRQs/DMA must be removed from the pool, the end user can use these PCI/PnP Setup options to remove the IRQ/DMA by assigning the option to the ISA/EISA setting. Onboard I/O is configurable by BIOS.

**Reserved memory Size**

This option specifies the size of the memory area reserved for legacy ISA adapter cards.

**Reserved memory Address**

This option specifies the beginning address (in hex) of the reserved memory area. The specified ROM memory area is reserved for use by legacy ISA adapter cards.

**5.7 PERIPHERAL SETUP**

This section is used to configure peripheral features.

AMIBIOS SETUP - PERIPHERAL SETUP (C) 1998 American Megatrends, Inc. All Rights Reserved		
OnBoard FDC	Auto	Available Options : Auto Disabled Enabled
OnBoard Serial Port1	Auto	
OnBoard Serial Port2	Auto	
OnBoard Parallel Port	Auto	
Parallel Port Mode	Normal	ESC:Exit ↑ ↓:Sel PgUp/PgDn:Modify F2/F3:Color
Parallel Port IRQ	Auto	
Parallel Port DMA Channel	N/A	
OnBoard PCI IDE	Enabled	
Primary Master Prefetch	Enabled	
Primary Slave Prefetch	Enabled	

**Figure 5-7 BIOS: Peripheral Setup**

**OnBoard FDC**

This option enables the floppy drive controller on the AR-B1542.

**OnBoard Serial Port**

This option enables the serial port on the AR-B1542.

**OnBoard Parallel Port**

This option enables the parallel port on the AR-B1542.

**Parallel Port Mode**

This option specifies the parallel port mode. ECP and EPP are both bi-directional data transfer schemes that adhere to the IEEE 284 specifications.

**Parallel Port DMA Channel**

This option is only available if the setting for the parallel Port Mode option is ECP.

**OnBoard PCI MASTER/SLAVE Prefetch**

This option specifies the onboard IDE controller channels that will be used.

## 5.8 AUTO-DETECT HARD DISKS

This option detects the parameters of an IDE hard disk drive, and automatically enters them into the Standard CMOS Setup screen.

## 5.9 PASSWORD SETTING

This BIOS Setup has an optional password feature. The system can be configured so that all users must enter a password every time the system boots or when BIOS Setup is executed. User can set either a Supervisor password or a User password.

Select the appropriate password icon (Supervisor or User) from the Security section of the BIOS Setup main menu. Enter the password and press [Enter]. The screen does not display the characters entered. After the new password is entered, retype the new password as prompted and press [Enter].

If the password confirmation is incorrect, an error message appears. If the new password is entered without error, press [Esc] to return to the BIOS Main Menu. The password is stored in CMOS RAM after BIOS completes. The next time the system boots, you are prompted for the password function is present and is enabled.

Enter new supervisor password:

## 5.10 LOAD DEFAULT SETTING

This section permits users to select a group of settings for all BIOS Setup options. You not only can use these items to quickly set system configuration parameters, but also can choose a group of settings that have a better chance of working when the system is having configuration related problems.

### 5.10.1 Auto Configuration with Optimal Setting

The user can load the optimal default settings for the BIOS. The Optimal default settings are best-case values that should optimize system performance. If CMOS RAM is corrupted, the optimal settings are loaded automatically.

Load high performance setting (Y/N) ?

### 5.10.2 Auto Configuration with Fail Safe Setting

The user can load the Fail-Safe BIOS Setup option settings by selecting the Fail-Safe item from the Default section of the BIOS Setup main menu.

The Fail-Safe settings provide far from optimal system performance, but are the most stable settings. Use this option as a diagnostic aid if the system is behaving erratically.

Load fail safe settings (Y/N) ?

## 5.11 BIOS EXIT

This section is used to exit the BIOS main menu. After making your changes, you can either save them or exit the BIOS menu and without saving the new values.

### 5.11.1 Save Settings and Exit

This item is in the <Standard CMOS Setup>, <Advanced CMOS Setup>, <Advanced Chipset Setup> and the new password (if it has been changed) will be stored in the CMOS. The CMOS checksum is calculated and written into the CMOS.

As you select this function, the following message will appear at the center of the screen to assist you to save data to CMOS and Exit the Setup.

Save current settings and exit (Y/N) ?

### 5.11.2 Exit Without Saving

When you select this option, the following message will appear at the center of the screen to help to abandon all the modified data and Exit Setup.

Quit without saving (Y/N) ?

### 5.12 BIOS UPDATE

The BIOS program instructions are contained within computer chips called FLASH ROMs that are located on your system board. The chips can be electronically reprogrammed, allowing you to upgrade your BIOS firmware without removing and installing chips.

The AR-B1542 provides FLASH BIOS update function for you to easily upgrade newer BIOS version. Please follow the operating steps for updating new BIOS:

**Step 1:** Turn on your system and don't detect the CONFIG.SYS and AUTOEXEC.BAT files. ***The importance is that the system has to load the HIMEM.SYS on the memory in the CONFIG.SYS file.***

**Step 2:** Insert the FLASH BIOS diskette into the floppy disk drive.

**Step 3:** In the MS-DOS mode, you can type the AMIFLASH program.

```
A:\>FLASH634
```

**Step 4:** The screen will show the message as follow:

Enter the BIOS File name from which Flash EPROM will be programmed. The File name must and with a <ENTER> or press <ESC> to exit.

**Step 5:** And then please enter the file name to the box of <Enter File Name>. And the box of <Message> will show the notice as follow. In the bottom of this window always show the gray statement.

Flash EPROM Programming is going to start. System will not be usable until Programming of Flash EPROM is successfully complete. In case of any error, existing Flash EPROM must be replaced by new program Flash EPROM.

**Step 6:** As the gray statement, press the <Y> key to updating the new BIOS. And then the <Message> box will show the <Programming Flash EPROM>, and the gray statement shows <Please Wait>.

**Step 7:** The BIOS update is successful, the message will show <Flash Update Completed - Pass>.

---

**NOTE:** 1. After turn on the computer and the system didn't detect the boot procedure, please press the [F5] key immediately. The system will pass the CONFIG.SYS and AUTOEXEC.BAT files. ***The importance is that the system has to load the HIMEM.SYS on the memory in the CONFIG.SYS file.***

2. The BIOS Flash disk is not the standard accessory. Now the onboard BIOS is the newest BIOS, if user needs adding some functions in the future please contact technical supporting engineers, they will provide the newest BIOS for updating.

3. The file of ***FLASH634.EXE had to Version 6.34.***

## 6. SPECIFICATIONS

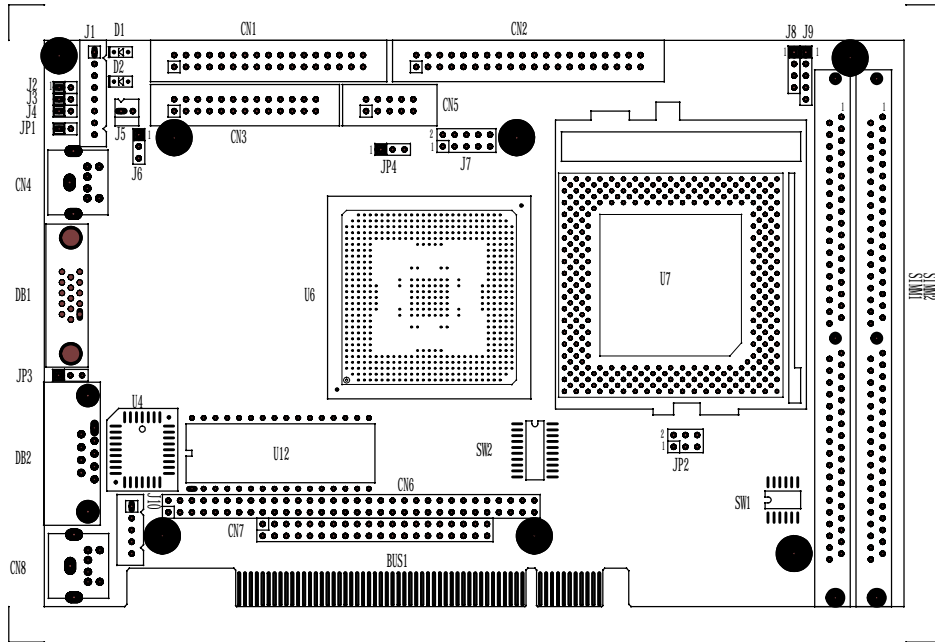
<b>CPU:</b>	Supports 75 to 450 Mhz CPU
<b>Chipset:</b>	SiS 5598
<b>Bus Interface:</b>	PICMG PCI and non-stack through PC/104 bus
<b>RAM Memory:</b>	Supports FPM/EDO RAM, 128 MB maximum (Two 72-pin SIMMs w/o DRAM)
<b>Cache Size:</b>	Synchronous pipe line burst SRAM 512KB
<b>VGA/LCD Display:</b>	4MB maximum shared memory (PCI bus, 1280X1024/high colors)
<b>HDC:</b>	Supports two IDE type 3.5" hard disk drives Supports LBA/Block mode access
<b>FDC:</b>	Supports two 5.25" or 3.5" floppy disk drives
<b>Parallel Port:</b>	1 bi-directional centronics type parallel port Supports SPP/EPP/ECP mode
<b>Serial Port:</b>	1 RS-232C and 1 RS-232C/RS-485
<b>Keyboard:</b>	PC/AT compatible with 6-pin mini-DIN connector located at bracket and 5-pin JAE connector
<b>USB:</b>	Built-in 2 port USB interface
<b>Watchdog:</b>	Programmable watchdog timer 3 to 42 seconds time interval
<b>Speaker:</b>	On-board Buzzer and external speaker
<b>Real Time Clock:</b>	BQ3287MT or compatible chips with 128 bytes data RAM
<b>BIOS:</b>	AMI Flash BIOS (256KB, including VGA BIOS)
<b>BUS Drive Cap.:</b>	8 TTL level loads maximum
<b>CE Design-In:</b>	Add EMI components to COM ports, parallel port, keyboard, and PS/2 mouse
<b>Indicator:</b>	Power LED, hard disk LED, and watchdog LED
<b>Power Req.:</b>	+5V & +12V, 3.5A maximum (base on Pentium-75)
<b>PC Board:</b>	8 layers, EMI considered
<b>Dimensions:</b>	185 mmX122mm (7.29"X4.80")



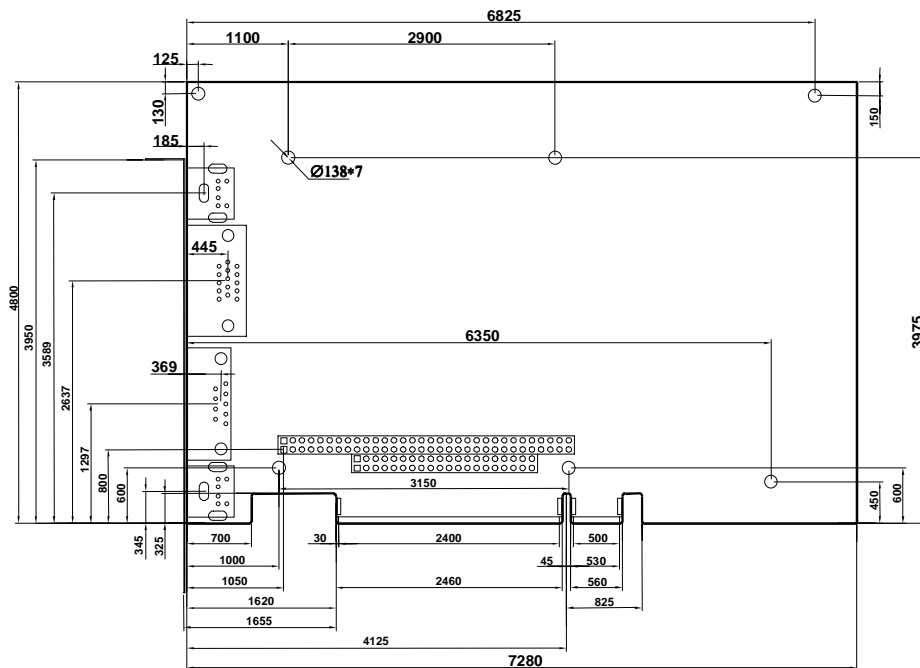


## 7. PLACEMENT & DIMENSIONS

### 7.1 PLACEMENT



### 7.2 DIMENSIONS



Unit: mil (1 inch = 25.4 mm = 1000 mil)

## 8. PROGRAMMING RS-485 & INDEX

### 8.1 PROGRAMMING RS-485

The majority communicative operation of the RS-485 is in the same of the RS-232. When the RS-485 proceeds the transmission which needs control the TXC signal, and the installing steps are as follows:

- Step 1:** Enable TXC
- Step 2:** Send out data
- Step 3:** Waiting for data empty
- Step 4:** Disable TXC

---

**NOTE:** Please refer to the section of the "Serial Port" in the chapter "System Control" for the detail description of the COM port's register.

#### (1) Initialize COM port

- Step 1:** Initialize COM port in the receiver interrupt mode, and /or transmitter interrupt mode. (All of the communication protocol buses of the RS-485 are in the same.)
- Step 2:** Disable TXC (transmitter control), the bit 0 of the address of offset+4 just sets "0".

---

**NOTE:** Communicates the AR-B1542 CPU card's DTR signal with the RS-485's TXC signal.

#### (2) Send out one character (Transmit)

- Step 1:** Enable TXC signal, and the bit 0 of the address of offset+4 just sets "1".
- Step 2:** Send out the data. (Write this character to the offset+0 of the current COM port address)
- Step 3:** Wait for the buffer's data empty. Check transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) are all sets must be "0".
- Step 4:** Disabled TXC signal, and the bit 0 of the address of offset+4 sets "0"

#### (3) Send out one block data (Transmit - the data more than two characters)

- Step 1:** Enable TXC signal, and the bit 0 of the address of offset+4 just sets "1".
- Step 2:** Send out the data. (Write all data to the offset+0 of the current COM port address)
- Step 3:** Wait for the buffer's data empty. Check transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) are all sets must be "0".
- Step 4:** Disabled TXC signal, and the bit 0 of the address of offset+4 sets "0"

#### (4) Receive data

The RS-485's operation of receiving data is in the same of the RS-232's.

**(5) Basic Language Example****a.) Initial 86C450 UART**

```
10 OPEN "COM1:9600,m,8,1"AS #1 LEN=1
20 REM Reset DTR
30 OUT &H3FC, (INP(%H3FC) AND &HFA)
40 RETURN
```

**b.) Send out one character to COM1**

```
10 REM Enable transmitter by setting DTR ON
20 OUT &H3FC, (INP(&H3FC) OR &H01)
30 REM Send out one character
40 PRINT #1, OUTCHR$
50 REM Check transmitter holding register and shift register
60 IF ((INP(&H3FD) AND &H60) >0) THEN 60
70 REM Disable transmitter by resetting DTR
80 OUT &H3FC, (INP(&H3FC) AND &HEF)
90 RETURN
```

**c.) Receive one character from COM1**

```
10 REM Check COM1: receiver buffer
20 IF LOF(1)<256 THEN 70
30 REM Receiver buffer is empty
40 INPSTR$=""
50 RETURN
60 REM Read one character from COM1: buffer
70 INPSTR$=INPUT$(1,#1)
80 RETURN
```

## 8.2 INDEX

Name	Function	Page
CN1	FDD port connector	3-15
CN2	Hard disk (IDE) connector	3-14
CN3	Parallel port connector	3-15
CN4	PS/2 Mouse Connector	3-14
CN5	RS-232 connector COM-B	3-17
CN6	64-pin PC/104 connector bus A & B	3-11
CN7	40-pin PC/104 connector bus C & D	3-11
CN8	Keyboard connector	3-13
DB1	CRT connector	3-20
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	COM-B RS-232C / RS-485 select	3-16
	D.O.C. memory address select	3-24
D3	Power LED	
D5	Watchdog LED	

Note:

If the content in Setting is inconsistent with CD-ROM. Please refer to the Setting as priority.