VMIVME-6005
Octal ARINC-429 Intelligent Communications Controller

- Eight transmit/sixteen receive channels
- Data rates 100 or 12.5 Kbits/s
- Simple memory-mapped command-response user interface
- 16 MHz 68000 I/O processor
- 64 Kbyte operational firmware/128 Kbyte local SRAM
- Supports ARINC-429 hardware-in-the-loop processing
- Supports ARINC-429 SDI/label sorting for eight receive channels
- Interrupt-coupled interface with status flags between I/O processor and VME host
- Programmable VMEbus interrupts and VMEbus interrupt vectors
- Programmable loopback self-test capability for each ARINC channel
- Extensive on-board diagnostic capability
- A32 and A24 slave VME interface
- D32/D16/D8 (EO) data transfer capability
- Double height standard Eurocard form factor
- VMEbus compatible ANSI/IEEE 1014-1987 IEC 821 and 297

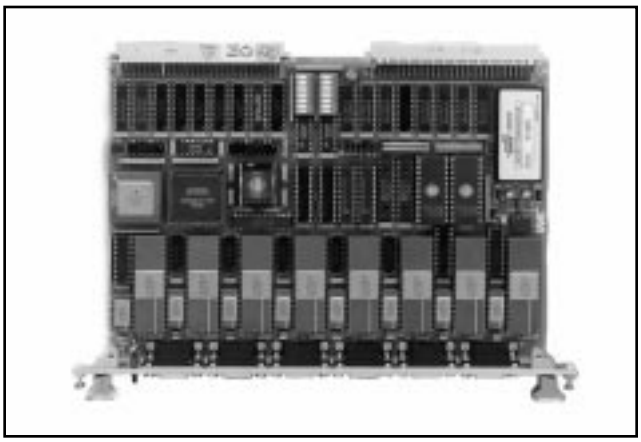
PRODUCT OVERVIEW — The VMIVME-6005 is a fully integrated communications controller providing VMEbus access to eight ARINC-429 high-speed serial interfaces. Each ARINC-429 interface is buffered: up to 255 32-bit words may be queued for transmission and each receiver has multiple 255 character buffers. ARINC-429 SDI/Label sorting may be commanded for eight receive channels with 1,024 character bins per channel. The 68000 I/O processor off-loads from the VMEbus the task of servicing the ARINC transceivers and managing the character buffers. The I/O processor communicates with the VME host through shared buffer memory, flags, and (optional) interrupts.

The VMIVME-6005 has an A32/A24 VME slave interface capable of D32, D16, and D8(EO) basic data transfers. The board may be jumper-configured to respond to supervisory, nonprivileged, or both supervisory and nonprivileged VME data transfers. The VMEbus base address of the VMIVME-6005 is configured with DIP switches to occupy a single 64 Kbyte block of memory.

The front panel of the VMIVME-6005 features six shielded DB-9 connectors for interface to the eight ARINC-429 transmit channels and sixteen ARINC-429 receive channels. Also included on the front panel, is a board reset switch and a health/status LED indicator. Transmitter line driver power is derived from VMEbus +5 V, although additional drive capability may be obtained from an external ±15 V source.

TECHNICAL DESCRIPTION — The VMIVME-6005 has five user programming interfaces:

a. Board ID buffer
b. Command/status interface
c. VME interrupt interface
d. Character buffers and offset pointers
e. Word count variables



The board ID buffer contains information about the board type, category, manufacturing options, revision level, and other information unique to the VMIVME-6005.

The Command Interface is a memory location which interrupts the SLAVE I/O processor when written to by the user. The code written to the Command interface instructs the SLAVE that either the ARINC-429 communication channels are to be set up, one of the ARINC-429 TX buffers contains new data to be transmitted, one of the RX buffers has been serviced, or self-test is to be performed. The Status Interface consists of four 8-bit read-only buffers: Slave I/O Processor Status, Receiver A Buffer Status, Receiver B Buffer Status, and Transmitter Buffer Status. These status buffers are updated by the Slave I/O processor.

The VME Interrupt Interface allows the user to specify an IRQ level and 8-bit interrupt vector to each of the ARINC-429 TX and RX buffers. At reset, the VME Interrupt Interface is quiescent and must be initialized by the Host.

Ordering Options

Nov. 12, 1993 800-006005-000 D		A	B	C	–	D	E	F
VMIVME-6005	–			0	–			

A =
0 = 8 Transmitters and 16 Receivers
1 = 4 Transmitters and 8 Receivers
2 = 1 Transmitter and 2 Receivers

B =
0 = All 100 Kbit/s
1 = All 12.5 Kbit/s
2 = 1/2-100 Kbit/s, 1/2 - 12.5 Kbits/s (Note 1)

C = 0 (Option reserved for future use)

Note

1. Not available for one transmitter and two receivers option. ∴ Option "-220" is not supported.

For Ordering Information, Call:
1-800-322-3616 or 1-256-880-0444 • FAX (256) 882-0859
E-mail: info@vmic.com Web Address: www.vmic.com
Copyright © May 1991 by VMIC
Specifications subject to change without notice.

Once the user has commanded the SLAVE to set up the VME Interrupt Interface, the SLAVE will interrupt the user whenever an RX buffer contains new data or when a TX buffer has been transmitted. The user may bypass this interrupt protocol by disabling all interrupt control words and polling the buffer Status interface.

The buffer memory is arranged as 255 sequential 32-bit longwords for each RXA, RXB, and TX channel of the ARINC-429 interface. Both the user and the SLAVE I/O processor may modify the buffer memory by following the buffer protocols. The buffer offset pointers are maintained by the slave.

The Word Count variables are 16-bit quantities which represent the number of 32-bit longwords contained in each buffer. There is a word count variable corresponding to each RXA, RXB, and TX ARINC-429 channel. Both the user and the SLAVE I/O processor may alter the Word Count variables following the buffer protocols.

TRANSMIT BUFFER PROTOCOL — The USER places a sequence of one or more 32-bit ARINC-429 words in the TX buffer, sets the Word Count variable to the number of 32-bit ARINC-429 words, and then asserts the TxReady command to the SLAVE. The SLAVE responds to the TxReady interrupt by moving the message words to the designated ARINC-429 transmitter. When the message is completely transmitted, the SLAVE clears that TX buffer status bit and, if enabled, asserts the TxDone interrupt back to the USER. The USER will not modify the TX buffer, word count variable, or TX buffer status until the SLAVE resets the TX buffer status, indicating the ARINC-429 words have been transmitted.

RECEIVE BUFFER PROTOCOL — For each ARINC-429 receiver, up to 255 characters are buffered in sequence. The SLAVE services the ARINC-429 receiver, places the 32-bit longword into the RX buffer, and then updates the number of 32-bit longwords into the word count variable. When the specified number of characters have been stored in the buffer, the SLAVE asserts the RxReady interrupt to the USER. The USER responds to the RxReady interrupt by reading the RX record in the buffer, and then asserting the RxDone interrupt back to the SLAVE. While the RX buffer status bit is set for a particular ARINC-429 RX buffer, the SLAVE I/O processor may continue to receive data from that channel and store the data into SLAVE local memory. Additional characters may be buffered by the SLAVE while the USER is unloading the shared RX buffer memory.

PIPELINE BUFFER PROTOCOL — Hardware-in-the-loop simulation is supported by the VMIVME-6005 with the Pipeline Protocol. Any of the sixteen ARINC-429 receivers may be paired with any of the eight ARINC-429 transmitters in pipeline fashion. A three-buffer queue allows the slave RX process to be filling one buffer, the VME host to be accessing the previous receive buffer, and the slave TX process to be sending the previous VME-accessed buffer. In this manner, the ARINC-429 data stream may be observed and modified by the VME host.

SDI/LABEL SORTING PROTOCOL — The VMEbus host may command the VMIVME-6005 to configure eight receivers for ARINC-429 SDI/Label sorting. In this mode, I/O processing is enabled for only eight receivers and pipeline mode is disabled. For each incoming character, the SDI code is appended to the label code to form a 10-bit address which is then adjusted for longword offset. The received character is then placed into one of 1,024 buffer bins. These sorting bins are static locations which may be interrogated by the VMEbus host at any time. The word count variables indicate the number of characters to be received before the RxReady interrupt is asserted, if enabled.

LABEL-CODE-ONLY SORTING MODE — The VMIVME-6005 supports sorting of ARINC-429 characters into a buffer with 256 character bins: only the eight-bit label code is used to create an offset address into the buffer. Just as with SDI/Label Sorting Protocol, the VMEbus host may command the VMIVME-6005 to configure up to eight receivers for Label-Code-Only Sorting. The eight RXA receivers may be individually configured for either SDI/Label Sorting or Label-Code-Only Sorting in any combination, since the sorting buffer locations remain static. The word count variables indicate the number of characters to be received before the RxReady interrupt is asserted, if enabled.

INTERRUPT-ON-LABEL-COMPARISON MODE — In either of the VMIVME-6005 Sorting modes, the user may choose a specific SDI/Label code to compare all incoming ARINC-429 characters against. When a received ARINC-429 character has an SDI/Label code (or just Label code, at the case may be) which matches the comparison value, the VMEbus interrupt associated with the receiver sorting buffer is asserted. This interrupt-on-label-comparison mode precludes the existing buffer limit count interrupt; when the buffer limit count is specified to be zero, the interrupt-on-label-comparison mode is enabled. As with the existing sorting modes, interrupt-on-label- comparison is available only for the eight RXA channels.

HARDWARE DESCRIPTION — The block diagram of the VMIVME-6005 Octal ARINC-429 Interface is shown in Figure 1. The VMIVME-6005 hardware may be partitioned into four functional groups: ARINC-429 bus interfaces, Slave I/O processor with firmware and support logic, control and record buffer memory, and VMEbus interface logic. Each functional group will be briefly described.

a. The ARINC-429 communication protocol is supported by eight transceivers compatible with the Harris HS-3282/HS-3182 chip set. Each chip set has an ARINC-429 transmitter, dual receiver, and an ARINC-429 transmit line driver.

b. The Slave I/O processor is a 16 MHz 68000 CPU with associated decode/timing logic and 64 kbytes of EPROM firmware. The CPU executes code copied into a 64 Kbyte block of SRAM not accessible from the VMEbus I/F. The ARINC-429 interfaces are serviced with prioritized interrupts and status flags.

c. The control and character buffer memory is a 64 Kbyte block of the slave I/O processor SRAM accessible from the VMEbus I/F. This user memory block contains the VMEbus interrupt control bytes, VMEbus interrupt vectors, RX/TX status flags, RX/TX word counts, and the RX/TX buffers. The VMEbus data interface to this memory may be D32, D16, or D8 (EO).

d. The VMEbus Slave I/F logic includes the Bus Interrupter Module, latches, comparators, transceivers, and control logic. The A24/A32 base address is configured by octal DIP switch blocks and jumpers.

INTERFACES

VMEbus Slave: A32:A24:D32:D16:D8(EO)

Commercial Airline: Eight ARINC-429 transmit and sixteen ARINC-429 receive channels

LED: A Status LED (red) is illuminated at power up and extinguished upon successful diagnostic execution

PHYSICAL/ENVIRONMENTAL

Length: 233.4 mm

Width: 160.0 mm

Depth: 19.2 mm

Weight: 20.0 oz

Operating: 0 to +55 °C (with 200 linear ft/min. airflow)
0 to 90 percent humidity (noncondensing)

Storage: -40 to + 85 °C
0 to 95 percent humidity (noncondensing)

68000 CPU

Address: 24 bits

Data: 8, 16 bits

Clock: 16 MHz

MEMORY

EPROM: 64 Kbyte

Static RAM: 128 Kbyte

ELECTRICAL POWER REQUIREMENTS

+5 VDC at 3.5 A

Optional Power Source:
±15 VDC at 400 mA
VMEbus P2 connector

TRADEMARKS

The VMIC logo is a registered trademark of VMIC. Other registered trademarks are the property of their respective owners.

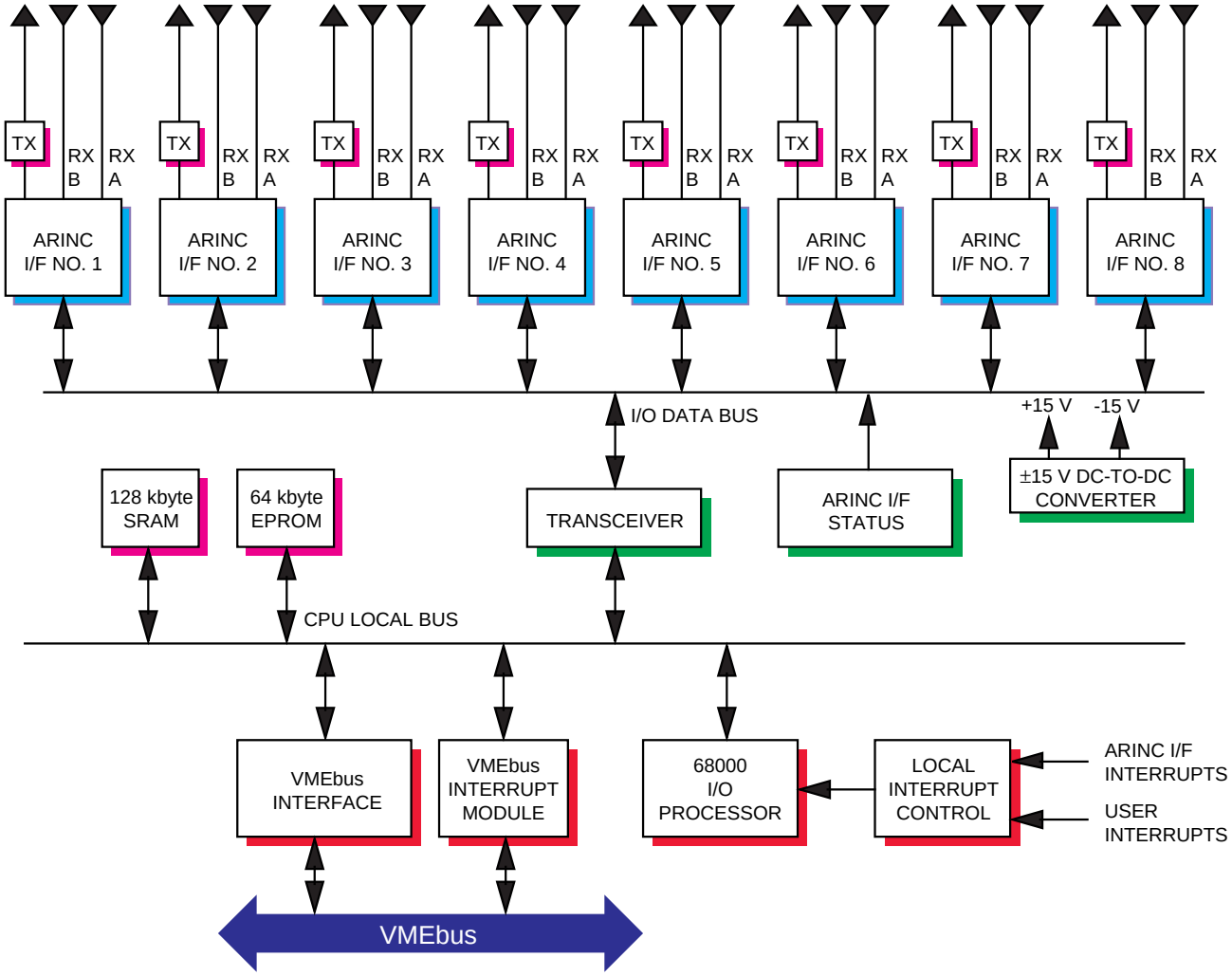


Figure 1. Octal ARINC-429 Interface