VMIVME-9150

IIOC Communications Controller VMEbus Host Communications Link for Multiple Reflective Memory Intelligent I/O Controllers

- Single host communications link controls multiple RM Intelligent I/O Controllers (IIOCs)
- Single point fault detection and isolation
- Minimizes host overhead
  - — Data buffers may contain points of all I/O types for multiple controllers
  - — Simplifies host data transfers
- High-speed host interface using RM or Ethernet
- Extensive host software support package
- Local I/O exercising support
- Slave chassis power down support

IIOC COMMUNICATIONS CONTROLLER — The IIOC Communications Controller (IIOC-CC) is a high-performance interface for linking multiple RM IIOCs to a single host computer. An optional standby host is also supported. Either host can drive the IIOC-CC; however, simultaneous operations from both hosts are not supported. The IIOC-CC provides high I/O data rates for very high I/O point count systems by allowing multiple VMIC IIOCs to operate independently. The IIOC-CC supports the VMIC VMIVME-9064/32 Reflective Memory-type IIOC.

A typical distributed IIOC system utilizing the IIOC-CC is shown in Figure 1. The IIOC-CC communicates with the IIOC subsystems via VMIC's high-speed RM. The RM concept provides a very fast and efficient way of sharing data across distributed VMEbus computer systems.

VMIC's RM interface allows data to be shared between VMEbus systems (nodes) at rates up to 30 Mbyte/s. Each RM board is configured with on-board SRAM. The local SRAM provides fast Read access times to stored data. Writes are stored in local SRAM and broadcast over a high-speed network to other RM nodes. The transfer of data between nodes is software transparent, so no I/O overhead is required. Transmit and Receive FIFOs buffer data during peak data rates to optimize single board computer (SBC) and bus performance to maintain high data throughput.

The IIOC-CC includes a Pentium® or Motorola processor based SBC with VMIC firmware and a 21-slot 6U chassis assembly. A wide variety of backplanes and power supplies are available to support specific customer requirements. Systems can also be configured as shown in Figure 2 to minimize rack space and reduce I/O subsystem cost.

HOST SOFTWARE SUPPORT PACKAGE — An extensive IIOC-CC Host Software Support Package (HSSP) is available that includes an I/O Point Manager, a Configuration Downloader, a Report Generator Utility, and a set of Real-Time Interface Software Modules. These tools allow the user to configure, document and program the IIOC subsystems via the IIOC-CC in a manner that minimizes errors and facilitates changes. All source code is available to the user to allow maximum programming flexibility.

PHOTO NOT AVAILABLE

IIOC SUBSYSTEM CONFIGURATION AND REAL-TIME OPERATION — The IIOC-CC supports a command from the host to select an IIOC subsystem for configuration and initialization. In order to configure a subsystem, the host first sends the command to select that IIOC subsystem. The host then downloads configuration data to the IIOC-CC which then configures the currently selected IIOC subsystem. After each IIOC subsystem has been configured, a single command may transfer input or output data used by all subsystems. In real-time, the host transfers data to and from the IIOC-CC without regard to the IIOC subsystems.

Ordering Options

June 23, 2003 800-009150-000 J	A	B	C	–	D	E	F
VMIVME-9150 –				–	0	0	0

ABC =
100 = Reserved
200 = Reserved
300 = Reserved
301 = 25.0 MHz Motorola M162P-242 (68040)
302 = 25.0 MHz Motorola M162PA-252SE (68040)
400 = Reserved
589 = 233 MHz Pentium, 64 Mbyte DRAM On-Board, Ethernet, Fast Ethernet
DEF = 000 (Options reserved for future use)

Note

Option -589 supports only Ethernet and Fast Ethernet host connectivity.

For Ordering Information, Call:
1-800-322-3616 or 1-256-880-0444 • FAX (256) 882-0859
E-mail: info@vmic.com Web Address: www.vmic.com

INTELLIGENT I/O CONTROLLER EXERCISER — The IIOC-CC provides the capability to drive the IIOCs from the communications controller (CC) without a host computer from simple menu selections.

The IIOC exerciser feature allows most of the functionality of the IIOC to be demonstrated. The IIOC-CC queries each IIOC for I/O boards present and automatically configures each IIOC. All channels on all I/O boards are configured with default data conversion types which may be changed by the user. I/O command lists are constructed automatically and the user may select the frame rate in hertz to perform the real-time I/O. The program can display and modify the digital, analog, and synchro output data being sent to an IIOC in real-time. Input data received from an IIOC may also be displayed. All channels on all the boards are exercised.

SLAVE IIOC CHASSIS POWER DOWN SUPPORT — The IIOC-CC and VMIVME-9064/32 support an individual chassis maintenance technique that allows the user to remove power from individual remote slave chassis connected to each VMIVME-9064/32 IIOC. The following steps provide an overview of the individual chassis power down scheme.

From the VMIVME-9150 control terminal, through a menu operation, the user requests that I/O on a specific VMIVME-9064/32 subcontroller be suspended so that one or more of the subcontroller's slave chassis may be powered down. This causes the following actions by the VMIVME-9150: the VMIVME-9150 stops I/O associated with the VMIVME-9064/32 subcontroller, commands the VMIVME-9064/32 to purge configuration, causing the VMIVME-9064/32 to be idle. The user is then informed that I/O is suspended so the chassis can now be powered down.

The chassis is now powered down without affecting the other VMIVME-9064/32 subcontrollers but its I/O is temporarily suspended. Through another menu selection, the VMIVME-9150 is notified by the user that I/O is to be resumed, possibly with missing I/O boards. The VMIVME-9150 then performs the following: the VMIVME-9150 commands the VMIVME-9064/32 to perform an I/O sizing and enable configuration of missing boards. The VMIVME-9150 commands the VMIVME-9064/32 to reconfigure using configuration data saved from previous download. The VMIVME-9150 then resumes the I/O scan operations on the VMIVME-9064/32 subcontroller.

When it is time for the chassis to be powered up again, a similar sequence is performed as above to suspend operations only on one VMIVME-9064/32, power up the chassis, reconfigure the VMIVME-9064/32, and resume scan operations. The interruption of I/O for the VMIVME-9064/32 subcontroller could be as short as 30 seconds, depending on the amount of time between the interactions at the VMIVME-9150 control terminal and the power down operations.

NOTE: Only available when using VMIVME-5550 Reflective Memory cards.

INTELLIGENT I/O CONTROLLER SUBSYSTEM — VMIC's RM IIOC combines the intelligence to ease integration and simplify maintenance with the power to significantly reduce the impact of real-time I/O on your host computer resources. The IIOC provides a high-density, high-throughput, low-cost solution to the data acquisition and control problem by offloading the I/O scanning, scaling computation, and engineering unit conversion tasks from host computer computational resources.

The IIOC subsystem supports a variety of VMIC's digital, analog and synchro/resolver I/O boards. Each I/O board is designed with extensive Built-in-Test capability and a front panel Fail LED to enable quick fault detection and isolation. The IIOC provides both offline and real-time testing for detecting and isolating failures on these products.

The processing capabilities of the 32-bit microprocessor provides extensive unit conversions for all I/O types, and interprets and formats the I/O data in host data formats. Digital conversions are provided to represent data as bit, byte, word, or longword logicals in host logical data formats or grouped together in variable width bit fields. Analog data may be represented in raw binary formats (offset binary and two's complement) or the host floating-point format for conversions including unipolar and bipolar scaling, trigonometric functions, lookup tables, and up to third-order polynomial expansions. Synchro/resolver data may be represented as raw offset binary or converted to the host floating-point format for unipolar and bipolar scaling. The ability to configure each I/O point individually eases the integration effort by allowing the hardware interface to change without affecting the host simulation code. Only the affected configuration data file is modified.

The IIOC supports an optional user-friendly CRT-based control panel (ANSI standard terminal) that allows the Systems Integrator or maintenance technician to monitor all I/O points or to selectively freeze output points during real-time operation. While the system is offline, the user may examine or modify I/O points and initiate and control diagnostics. The control panel provides for the display of the current status of the system, errors found during real-time or off-line diagnostics, and the current

system hardware configuration. The control panel facilitates maintenance, test, integration, and checkout of the IIOC independent of a host computer system.

The VMIC real-time IIOC subsystem configuration is organized as shown in Figure 3. The central node of the I/O subsystem is the IIOC master chassis which is responsible for all I/O handler communications, CRT control, data format, off-line and real-time subsystem testing, engineering unit conversions, and communications with the satellite or slave chassis. System performance requirements will determine the number and type of I/O boards controlled by each IIOC in the distributed system. Each IIOC can support up to 11 slave chassis of 19 I/O boards, each with 32-bit data path VMEbus repeaters. Typical applications will require only two or three chassis including the master chassis for each IIOC subsystem. Long-line repeaters can be provided to allow slave chassis to be located up to 2,000 feet from the IIOC. Multidrop bus repeaters are available to reduce cable requirements and costs.

INTELLIGENT I/O CONTROLLER (IIOC) FIRMWARE*

- Diagnostic firmware
  - — Processor
  - — Local memory
  - — Global memory
  - — Local diagnostic control
  - — Error reporting
  - — Offline and real-time fault detection and isolation
- Diagnostic control
  - — Power up initialization
  - — Host initiated
  - — Local terminal control
- Failure reporting
  - — Front panel fail LEDs
  - — Local terminal option
  - — Host report
- Real-time firmware
  - — Extensive I/O data conversions
  - — I/O data transfers
  - — Real-time fault detection
  - — Synchro output step limiting
  - — Analog output step limiting
  - — Analog input smoothing

* For a detailed explanation of the performance, features, and operation of the IIOC, refer to the IIOC Family Instruction Manual (VMIC's Document No. 500-009000-000).

TRADEMARKS

I/O BOARD SUPPORT

The following VMIC I/O boards are supported:	Model No.
• Digital I/O boards	
— 64-bit high-voltage digital input	VMIVME-1110*
— 64-bit high-voltage and/or differential digital input	VMIVME-1111
— 128-bit high-voltage digital input board with Built-in-Test	VMIVME-1128
— 128-bit high-voltage filtered digital input	VMIVME-1129
— 64-bit optically isolated digital input	VMIVME-1150
— 64-bit high-voltage digital output	VMIVME-2120
— 128-bit voltage source digital output	VMIVME-2127
— 128-bit high-voltage digital output board with Built-in-Test	VMIVME-2128
— 64-bit high-current source digital output	VMIVME-2130
— 64-bit high-current sink/source digital output	VMIVME-2131
— 64-bit digital output relay board with Built-in-Test	VMIVME-2210
— 32-channel relay board	VMIVME-2232
— 64-bit TTL digital I/O	VMIVME-2510B
— 128-bit TTL-level digital output	VMIVME-2528 (4)
— 32-bit high-voltage digital output and 32-bit high-voltage digital input	VMIVME-2532A*
— 32-bit differential digital output	VMIVME-2533
— 32-bit high-voltage digital input and/or output with P2 I/O and Built-in-Test	VMIVME-2534
• Analog I/O boards	
— 12-bit ADC (jumper-selectable gain)	VMIVME-3100 (1)
— High-speed 12-bit ADC with autocal	VMIVME-3101 (1)
— 12-bit analog-to-digital converter, 48 inputs, and 2 D/A outputs	VMIVME-3111 (2)
— Scanning 12-bit analog-to-digital converter board with Built-in-Test	VMIVME-3113 (2, 3)
— High-resolution analog-to-digital converter board	VMIVME-3116 (2, 3)
— 8-channel, 16-bit resolution analog output board	VMIVME-4116 (2)
— 32-channel analog output board with Built-in-Test	VMIVME-4132 (2)
— 16-channel (S&H per channel) analog output board with 16 single-ended analog input multiplexer	VMIVME-4500A (2)
— 16-channel, 12-bit analog I/O board (AIO) with Built-in-Test on-board	VMIVME-4512 (2)
— 16-channel scanning analog I/O board with Built-in-Test and P2 I/O	VMIVME-4514 (2)
• Synchro/resolver boards	
— Dual-channel digital-to-synchro/resolver	VMIVME-4900
— Dual-channel digital-to-synchro/resolver with 5.0 VA option	VMIVME-4905
— Quad-channel synchro/resolver-to-digital converter	VMIVME-4911
• Serial I/O	
— Quad-channel serial I/O	VMIVME-6015

*The use of 5 ms filters on VMIVME-1110 digital input (DI) boards or on VMIVME-2532A digital input/output (DIO) boards require the use of a delay of 10 ms before DI scanning in the event the I/O service interrupt occurs during DI real-time testing. This delay is necessary to preclude erroneous real-time data because of filter capacitor discharge/charge time. By placing the transfer DI and scan DI commands at the beginning of the frame, the 10 ms may be absorbed by the processing of the other I/O types. VMIC offers a product (VMIVME-1111) which will allow the use of 5 ms filters without any real-time input service delay. A high-density (VMIVME-1128) version is also available.

1. Front panel inputs are not supported. (The VMIVME-3100 and -3101A require the use of VMIVME-4500As for analog input processing.)
2. Compatible with VMIC's 3V/5V signal conditioning assemblies. This interface capability allows these boards to digitize the following input signals: low-level voltage, AC voltage, thermocouple, RTD, current, frequency, strain gauge, LVDT, and high-level voltage.
3. Front panel inputs are supported.
4. Supported as a 128-bit output board only.

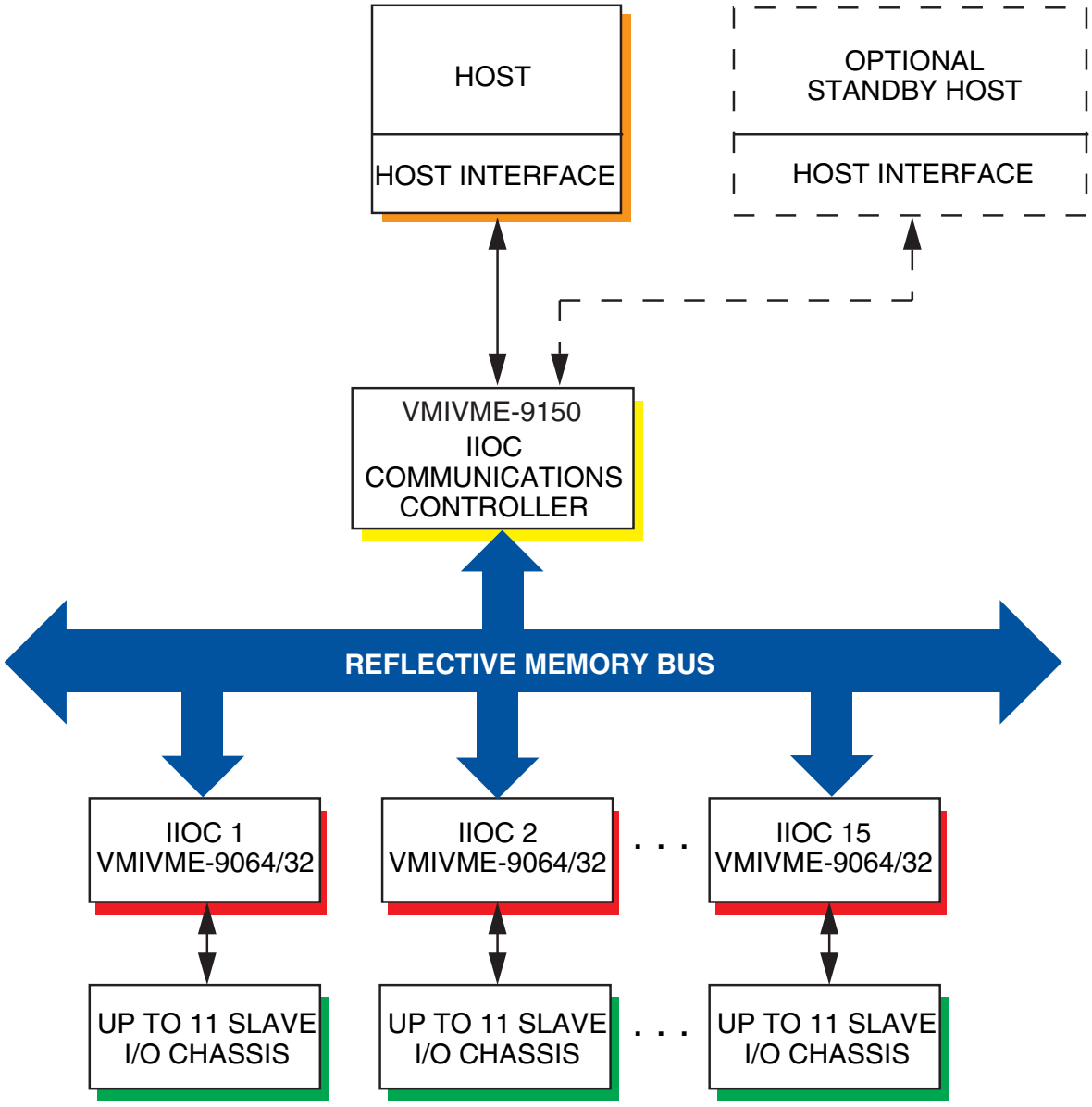

Figure 1. I/O Subsystem Configuration Based on Communications Controller

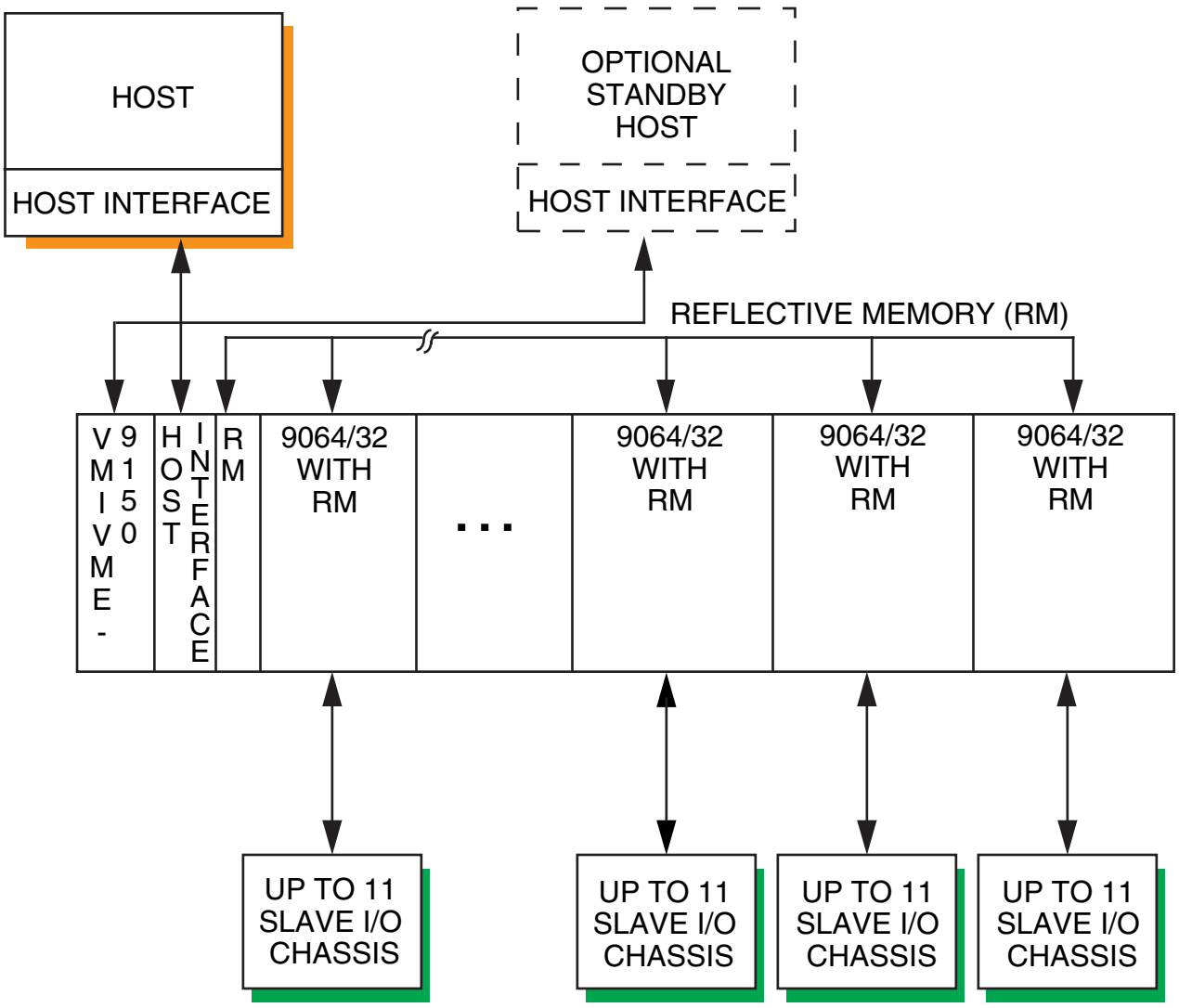

Figure 2. I/O Subsystem Configuration with IIOCs Collocated with the IIOC-CC (VMIVME-9150)

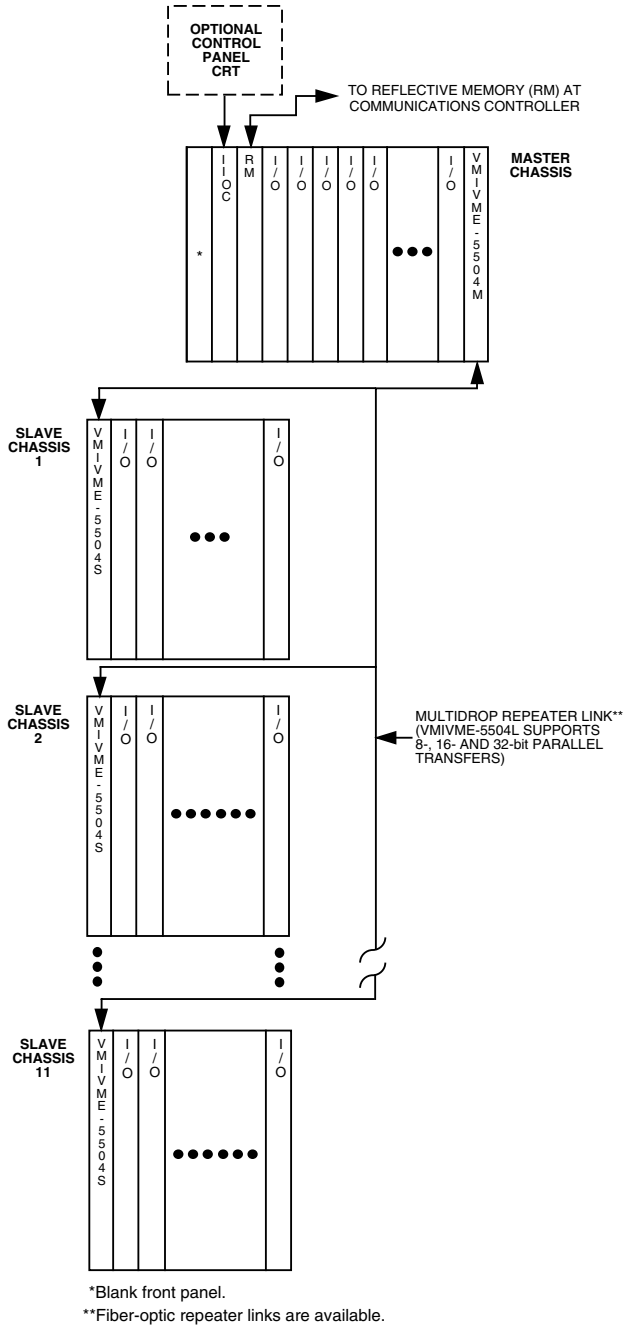

Figure 3. Intelligent I/O Controller Subsystem Block Diagram Using Multidrop Repeater Link