

HS-5210/5020

Half Pentium[®] MMX[™] VGA LAN

Half Size All-in-one with VGA Interface 100-Based Network
Supports DMA33 WDT DOC CTA USB IrDA
ISA Bus Industrial Single Board Computer

HS-5210V/5020V

Half Pentium[®] MMX[™] VGA I.S.B.

Half Size All-in-one with VGA Interface
Supports DMA33 WDT DOC CTA USB IrDA
ISA Bus Industrial Single Board Computer

HS-5210P/5020P

Half Pentium[®] MMX[™] I.S.B.

Half Size All-in-one Supports DMA33
WDT DOC CTA USB IrDA
ISA Bus Industrial Single Board Computer

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Contents

<i>HS-5210/5020</i>	1
<i>HS-5210V/5020V</i>	1
<i>HS-5210P/5020P</i>	1
GENERAL INFORMATION	3
1.1 MAJOR FEATURES.....	4
1.2 SPECIFICATIONS	5
1.3 DELIVERY PACKAGE.....	6
HARDWARE INSTALLATION	7
2.1 CAUTION OF STATIC ELECTRICITY	7
2.2 CAUTION ON UNPACKING AND BEFORE INSTALLATION.....	8
2.3 HS-5210/5020'S LAYOUT.....	9
2.4 QUICK LISTING OF JUMPERS.....	10
2.5 QUICK LISTING OF CONNECTORS	10
2.6 JUMPER SETTING DESCRIPTION.....	11
2.7 SETTING THE CPU OF HS-5210/5020.....	12
2.8 SYSTEM MEMORY DRAM.....	14
2.9 WATCH-DOG TIMER.....	14
2.10 VGA CONTROLLER.....	17
2.11 DISKONCHIP? ADDRESS SETTING	18
2.12 BIOS TYPE SELECTION.....	18
CONNECTION	19
3.1 THE FLOPPY DISK DRIVE CONNECTOR.....	19
3.2 PCI E-IDE DRIVE CONNECTOR.....	20
3.3 PARALLEL PORT CONNECTOR.....	21
3.4 SERIAL PORTS CONNECTORS	22
3.5 KEYBOARD CONNECTORS	23
3.6 POWER'S LED, KEY-LOCK AND RESET BUTTON.....	23
3.7 EXTERNAL SPEAKER.....	24
3.8 PS/2 MOUSE 6-PIN MINI-DIN CONNECTOR.....	24
3.9 VGA CONNECTORS	25
3.10 IR CONNECTOR.....	25
3.11 EXTRA POWER CONNECTOR	26
3.12 USB PORTS CONNECTOR	26

3.13 FAST ETHERNET CONNECTOR	27
AWARD BIOS SETUP	28
4.1 MAIN MENU	29
4.2 STANDARD CMOS SETUP.....	30
4.3 BIOS FEATURES SETUP.....	31
4.4 CHIPSET FEATURES SETUP.....	32
4.5 INTEGRATED PERIPHERALS.....	33
4.6 POWER MANAGEMENT SETUP.....	34
A BRIEF BROWSE OF 10/100 BASED-T LAN RTL-8139'S INSTALLATION SOFTWARE.....	35

Chapter-1

General Information

The HS-5020 is a ISA bus (HS-5210 for PISA bus) MMX™/Pentium® Industrial Single Board (I.S.B.) CPU card with features combine together to make it an ideal all-in-one industrial single board computer, enhanced I/O effects, VGA and NE2000 compatible Network interface. The model HS-5210P/5020P is based on HS-5210/5020' s features but without LAN on-board.

With on-board DMA33 of mode 4 to IDE drive interface architecture, the HS-5210/5020 supports with maximum 33.3 MB/sec in data transfer rating to 4 pieces IDE drive connection. Design with SiS598 UMA VGA, a new generation and memory share controller built-in. Up to share 4MB main memory and supports 1280 x 1024 64K colors & Virtual screen up to 2048 x 2048 resolutions.

The advanced ISA bus add-on connection of HS-5020 (PISA bus is for HS-5210) allows user could easily obtain ISA's full set signals from a small 16-bit ISA slot for suitable plug into a small size system with 8/16-bit operating. The HS-5210/5020 supports BEDO, EDO and FPM DRAM sockets. This gives you the flexibility of configuring your system from 1 to 128 MB DRAM by using the most economical SIMMs. It also provides two 72-pin SIMM sockets for its on-board system DRAM.

A single Flash chip holds the system BIOS, and you can change the Flash BIOS by the Utility Update. Advanced USB and IR ports also provide a faster data transmission. You can also use the DOS version of the "DiskOnChip? " socket by issuing commands from the DOS prompt without the necessity of other software supports up to 144MB.

The HS-5210/5020 features include a temperature-warning sensor installed under the CPU socket. The sensor monitors the CPU temperature and generates a warning buzzer in response to the temperature increases that may cause a system malfunctions.

If a non-expect program cause halts, the on-board watchdog timer will automatically reset the CPU or generate an interrupt. The watchdog is designed for pure hardware and doesn't need any arithmetical functions of a real-time clock chip. This ensures the reliability in an unmanned or standalone system.

1.1 Major Features

- ✂✂ ISA bus supported.
- ✂✂ Intel Pentium® CPU 75 300 MHz, AMD k5, k6,k6-2 333MHz, 350MHz
Cyrix 6x86, M2 300MHz, Intel MMX™, Socket 7 ZIF socket.
- ✂✂ SiS 5598 chipset.
- ✂✂ 100 base Network on board, NE2000 compatible. (HS-5210/5020
only).
- ✂✂ Ultra DMA33 Supported four fast PCI enhanced IDE drives (large hard
disks, CD-ROM, tape backup, etc.)
- ✂✂ Supports EDO or Fast Page DRAM up to 128 MB.
- ✂✂ PnP I/O address & IRQ selection
- ✂✂ On-board W83877 super I/O. Two high-speed serial RS-232 ports (with
16C550 UART 16-byte FIFO). One enhanced bi-directional parallel port
supports SPP/EPP/ECP.
- ✂✂ On-board keyboard and PS/2 Mouse connector.
- ✂✂ On-board SiS 5598 UMA VGA, a new generation and memory share
controller built-in. Up to share 4MB main memory and supports 1280 x
1024 64K colors & Virtual screen up to 2048 x 2048 resolutions.
- ✂✂ "DiskOnChip? " socket supports, memory size up to 144 MB.
- ✂✂ Switch Power Regulator.

1.2 Specifications

- ✂✂ **CPU:** Intel MMX/Pentium 75~300MHz, AMD k5, k6, k6-2 350MHz Cyrix 6x86,M2 300MHz.
- ✂✂ **Bus interface:** ISA bus / PISA bus
- ✂✂ **Chipset:** SiS 5598
- ✂✂ **Data bus:** 64-bit
- ✂✂ **Processing ability:** 64-bit
- ✂✂ **VGA Controller:** SiS 5598 chipset built in GUI/Video accelerator and 24 bit true color RAMDAC, new generation UMA architecture with CPU Bus/Data compression and share system memory up to 4MB.
- ✂✂ **VGA Resolution:** Resolutions up to 1280 x 1024 64K color and support virtual screen up to 2048 x 2048.
- ✂✂ **PCI Enhanced IDE interfaces:** Supports up to four IDE devices, support Ultra DMA/33, data transfer rate 33MB/Sec.
- ✂✂ **RAM memory:** Up to 128MB, uses two 72-pin SIMM sockets, supports BEDO, EDO and FastPage DRAM.
- ✂✂ **Cache memory:** 512KB Pipeline burst cache memory.
- ✂✂ **Ethernet:** RJ-45 100 based PCI Ethernet, Novell NE2000 compatible. Used RTL8139 Chipset.
- ✂✂ **Floppy disk drive interface:** Supports up to two floppy disk drives.
- ✂✂ **Parallel port:** One bi-directional parallel port. Supports SPP/ECP/EPP.
- ✂✂ **Serial ports:** Two RS-232 ports. Both use 16C550 UART with 16-byte FIFO.
- ✂✂ **BIOS:** AWARD PnP flash BIOS.
- ✂✂ **Watchdog timer:** Hardware circuit can be set by 1, 2, 10, 20, 110, or 220 seconds period Reset or NMI were generated when CPU did not periodically trigger the timer.
- ✂✂ **DMA channels:** 7
- ✂✂ **Interrupt levels:** 15
- ✂✂ **Keyboard:** 6-pin mini DIN connector or 5-pin header supports standard PC/AT keyboard.
- ✂✂ **Mouse:** 6-pin mini DIN connector support PS/2 standard mouse.
- ✂✂ **USB:** Supports 2 USB header.
- ✂✂ **IR interface:** Supports one IrDA TX/RX header.
- ✂✂ **Flash memory Disk:** Reserved socket for "DiskOnChip™", support up to 144MB Flash memory disk.
- ✂✂ **Extra power:** Supports 8-PIN extra power connector.
- ✂✂ **CMOS:** Real-time clock/calendar and battery backup by DS12B887 or

equivalent device.

- ~~✂~~ **Power supply voltage:** +5V (4.75 to 5.25V), +12V / -12V power supply.
 - ~~✂~~ **Max. Power requirement:** +5V @3.5A, +12V/-12V @20mA.
 - ~~✂~~ **Operating temperature:** 0~55°C (CPU need cooler)
 - ~~✂~~ **Board size:** 7.3"(L) x 4.8" (W) (185mm x 122mm)
-

1.3 Delivery Package

The delivery package of HS-5210/5020 includes all following items:

- #** HS-5210/5020 Industrial Single Board
- #** One Printer & COM2 Bracketed Flat Cable
- #** Two IDE port Flat Cables
- #** FDD port Flat Cable
- #** COM port Cable
- #** One PS/2 Keyboard to Standard Keyboard Cable
- #** VGA Utility Diskette (2 pcs)
- #** User' s Manual

Please contact with your dealer if any of these items are missing or damaged when purchasing. And please keep all parts of the delivery package with packing materials in case of you want to ship or store the product in feature.

Chapter-2

Hardware Installation

This chapter provides the information on how to install the hardware of HS-5210/5020. At first, please follow up sections 1.3, 2.1 and 2.2 in check the delivery package and carefully unpacking. Following after, the jumpers setting of switch, watchdog timer, and the DiskOnChip? address selection.

The CN15 only available of model HS-5210/5020, and CN16 only available of model HS-5210P/5020P.

2.1 Caution of Static Electricity

The HS-5210/5020 has been well package with an anti-static bag in protect its sensitive computer components and circuitry from the damage of static electric discharge.

Note: DO NOT TOUCH THE BOARD OR ANY OTHER SENSITIVE COMPONENTS WITHOUT ALL NECESSARY ANTI-STATIC PROTECTION.

You should follow the steps as following to protect the board in against the static electric discharge whenever you handle the board:

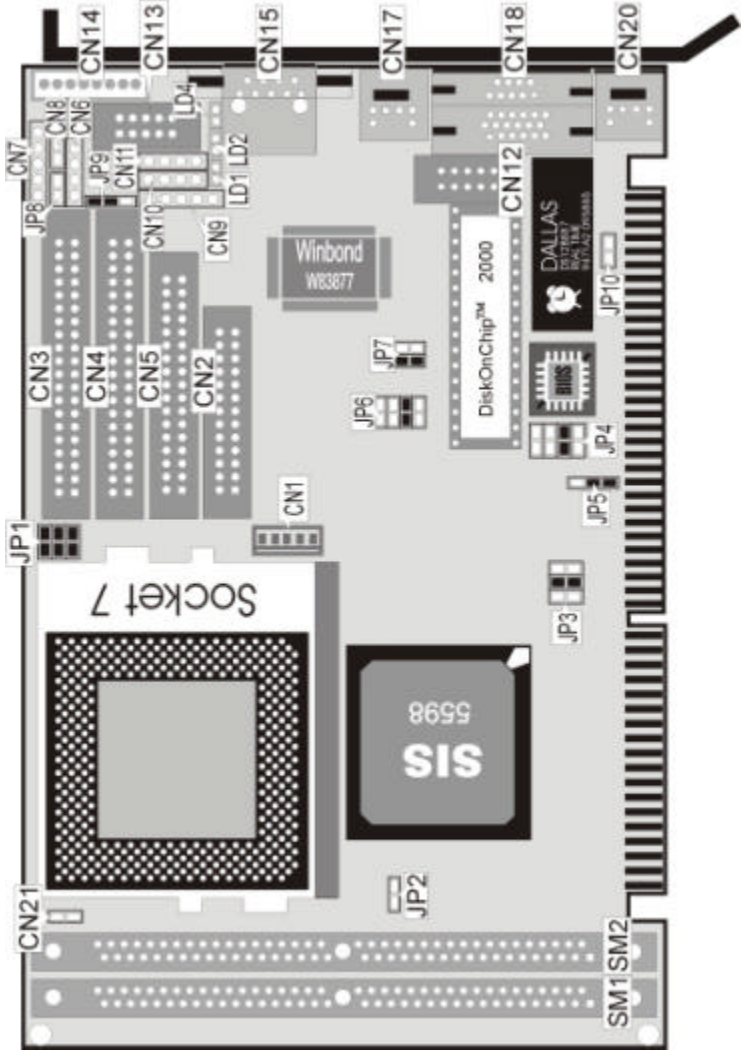
1. Please use a grounding wrist strap on whoever needs to handle the HS-5210/5020. Well clip the ALLIGATOR clip of the strap to the end of the shielded wire lead from a grounded object. Please put on and connect the strap before handle the HS-5210/5020 for harmlessly discharge any static electricity through the strap.
2. Please use anti-static pad for put any components or parts or tools on the pad whenever you work on them outside the computer. You may also in use the anti-static bag instead the pad. Please ask from your local supplier in help up your necessary parts on anti-static requirement.

2.2 Caution on Unpacking and Before Installation

First of all, please follow with all necessary steps of section 2.1 in protection the HS-5210/5020 from electricity discharge. With refer to section 1.3, please check the delivery package again with following steps:

1. Unpacking the HS-5210/5020, keep well storage of all packing material, manual and diskette etc. if has.
2. Is there any components lose or drop from the board? **DO NOT INSTALL IF HAPPENED.**
3. Is there any visual damaged of the board? **DO NOT INSTALL IF HAPPENED.**
4. Well check from your optional parts (i.e. CPU, SRAM, DRAM, ROM-Disk etc.) for completed setting all necessary jumpers setting to jumper pin-set and CMOS setup correctly. Please also reference to all information of jumpers setting in this manual.
5. Well check from your external devices (i.e. Add-On-Card, Driver Type etc.) for completed add-in or connection and CMOS setup correctly. Please also reference to all information of connector connection in this manual.
6. Please keep all necessary manual and diskette in a good condition for your necessary re-installation if you change your Operating System or whatever needs.

2.3 HS-5210/5020's Layout



2.4 Quick Listing of Jumpers

- JP1 — for CPU type setting
- JP2 — VGA Enable Selection
- JP3 — CPU Clock-in Select
- JP4 — WATCH-DOG Time-out period selection
- JP5 — Type setting of Flash BIOS
- JP6 — CPU's Vcore voltage level selection setting
- JP7 — for DiskOnChip™ address setting
- JP9 — WATCH-DOG Active Select
- JP10 — CMOS Data Clear

2.5 Quick Listing of Connectors

- CN1: 5P KEYBOARD CONNECTOR
- CN2: PARALLEL PORT
- CN3: 1st HDD (IDE) CONNECTOR
- CN4: 2nd HDD (IDE) CONNECTOR
- CN5: FDD CONNECTOR
- CN6: SPEAKER CONNECTOR
- CN7: KEYLOCK
- CN8: HDD LED
- CN9: IR CONNECTOR
- CN10: USB1 CONNECTOR
- CN11: USB0 CONNECTOR
- CN12: COM2 (HEADER 5x2)
- CN13: COM1 (HEADER 5x2)
- CN14: 8P POWER CONNECTOR
- CN15: RJ-45 NETWORK CONNECTOR (HS-5210/5020 only)
- CN16: COM1 (HS-5210P/5020P only)
- CN17: MINI-DIN 6-PINS MOUSE CONNECTOR (PS/2)
- CN18: EXTERNAL VGA CONNECTOR (DB15)
- CN20: MINI-DIN 6-PINS KEYBOARD CONNECTOR (PS/2)
- LD1, LD2, LD4: LAN' s LED INDICATOR CONNECTORs
- JP8: RESET BUTTON CONNECTOR

2.6 Jumper Setting Description

A jumper pin-set is **ON** as a shorted circuit with a plastic cap inserted over two pins. A jumper pin-set is **OFF** as a open circuit with a plastic cap inserted over one or no pin(s) between pins. The below figure 2.2 shows the examples of different jumper pin-set setting as **ON** or **OFF** in this manual.

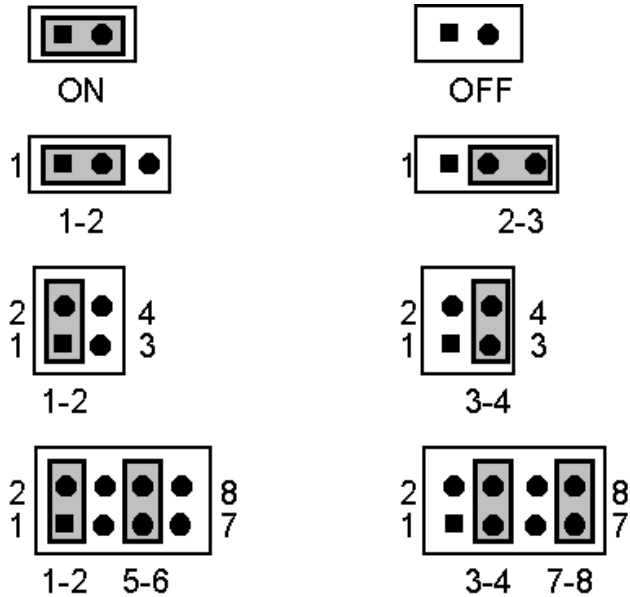


Figure 2.2

All jumper pin-set already has its default setting with the plastic cap inserted as ON, or without the plastic cap inserted as OFF. The default setting may reference in this manual with a "*" symbol in front of the selected item.

2.7 Setting the CPU of HS-5210/5020

The HS-5210/5020 provides all possibility in jumper setting for wide using all types of CPU with JP1 and JP3 setting.

The following table shows all possibility of the setting with JP3. The JP3 used to setting the System clock base rate. The System clock setting will preset the system operating clocking base rate. The setting of JP3 also shows the PCI Bus Clock rate in selection.

☞ System Clock select

JP3	System Clock	PCI Bus Clock
1-2, 3-4	50 MHz	25 MHz
OFF	55 MHz	27.5 MHz
1-2	60 MHz	30 MHz
3-4	*66.6 MHz	*33.3 MHz
1-2, 5-6	75 MHz	32 MHz
3-4, 5-6	83.3 MHz	32 MHz

*) : default setting

The JP1 sets the multi-times ratio of the CPU' s specification. Please reference to the following table for all type CPU in used.

☞ CPU' s Clock Ratio select

Clock Ratio			JP1		
Intel		AMD			
P54C	P55C	K6	5-6	3-4	1-2
2.5	2.5	*2.5	OFF	ON	ON
3.0	3.0	3.0	OFF	ON	OFF
2.0	2.0	2.0	OFF	OFF	ON
1.5	3.5	3.5	OFF	OFF	OFF
2.5	2.5	4.5	ON	ON	ON
3.0	3.0	5.0	ON	ON	OFF
1.5	2.0	4.0	ON	OFF	ON
2.5	3.5	5.5	ON	OFF	OFF

*) : default setting

Correspond to different type CPU, it is request to set JP6 for match the CPU's Vcore operating voltage. Here shows at below of the proper jumper settings for their respective Vcore at range 2.0V to 3.5V.

CPU Vcore Voltage Selection

CPU Vcore Voltage	JP6
2.0V	ALL OFF
2.1V	1-2
2.2V	3-4
2.3V	1-2, 3-4
2.4V	5-6
2.5V	1-2, 5-6
2.6V	3-4, 5-6
2.7V	1-2, 3-4, 5-6
2.8V	7-8
*2.9V	1-2, 7-8
3.0V	3-4, 7-8
3.1V	1-2, 3-4, 7-8
3.2V	5-6, 7-8
3.3V	1-2, 5-6, 7-8
3.4V	3-4, 5-6, 7-8
3.5V	1-2, 3-4, 5-6, 7-8

*) : default setting

The above default setting of JP1, JP3 and JP6 show a AMDK6-166(2.9V) CPU in used. (i.e. 66.6 x 2.5 ~ 166 MHz). Please contact with your CPU supplier for detail specification in correcting selected setting of JP1, JP3 and JP6.

2.8 System Memory DRAM

The HS-5210/5020 provides a wide range on-board DRAM memory by two pieces SIMM sockets (Bank0 & Bank1) to accept 1 MB, 2MB, 4MB, 8MB, 16MB, 32MB or 64MB. The SIMMs (Single In-Line Memory Modules) RAM request the access time should be 70 n-second or faster. The total capacity of the on board memory are between 2MB to 128MB.

See the figure on section 2.3 for get the identifying the banks. Please take notes that the memory capacity of both SIMMs should be the same.

The HS-5210/5020 requires **at least 2pcs of the RAM modules on SIMM socket.**

2.9 Watch-Dog Timer

There are three access cycles of Watch-Dog Timer as Enable, Refresh and Disable. The Enable cycle should proceed by READ PORT 443H. The Disable cycle should proceed by READ PORT 043H. A continue Enable cycle after a first Enable cycle means Refresh.

Once if the Enable cycle activity, a Refresh cycle is request before the time-out period for restart counting the WDT Timer's period. Otherwise, it will assume that the program operation is abnormal when the time counting over the period preset of WDT Timer. A System Reset signal to start again or a NMI cycle to the CPU comes if over.

The JP9 is using for select the active function of watch-dog timer in disable the watch-dog timer, or presetting the watch-dog timer activity at the reset trigger, or presetting the watch-dog timer activity at the NMI trigger.

JP9 : Watch-Dog Active Type Setting

JP9	DESCRIPTION
*1-2	System Reset
2-3	Active NMI
OFF	disable Watch-dog timer

JP4 : WDT Time - Out Period

PERIOD	1-2	3-4	5-6	7-8
*1 sec	OFF	OFF	ON	OFF
2 sec	OFF	OFF	ON	ON
10 sec	OFF	ON	OFF	OFF
20 sec	OFF	ON	OFF	ON
110 sec	ON	OFF	OFF	OFF
220 sec	ON	OFF	OFF	ON

The Watch-dog timer is disabled after the system Power-On. The watch-dog timer can be enabled by a Enable cycle with reading the control port (443H), a Refresh cycle with reading the control port (443H) and a Disable cycle by reading the Watch-dog timer disable control port (043H). After a Enable cycle of WDT, user must constantly proceed a Refresh cycle to WDT before its period setting comes ending of every 1, 2, 10, 20, 110 or 120 seconds. If the Refresh cycle does not active before WDT period cycle, the on board WDT architecture will issue a Reset or NMI cycle to the system.

The Watch-Dog Timer is controlled by two I/O ports.

443H	I/O Read	The Enable cycle.
443H	I/O Read	The Refresh cycle.
043H	I/O Read	The Disable cycle.

The following sample programs showing how to Enable, Disable and Refresh the Watch-dog timer:

```

WDT_EN_RF      EQU    0443H
WDT_DIS        EQU    0043H

WT_Enable      PUSH   AX                ; keep AX DX
                PUSH   DX
                MOV    DX,WDT_EN_RF    ; enable the watch-dog timer
                IN     AL,DX
                POP    DX                ; get back AX, DX
                POP    AX
    
```

RET

```

WT_Refresh      PUSH  AX           ; keep AX, DX
                PUSH  DX
                MOV   DX,WDT_ET_RF ; refresh the watch-dog timer
                IN    AL,DX
                POP   DX           ; get back AX, DX
                POP   AX
                RET

WT_DISABLE      PUSH  AX
                PUSH  DX
                MOV   DX,WDT_DIS   ; disable the watch-dog timer
                IN    AL,DX
                POP   DX           ; get back AX, DX
                POP   AX
                RET

```

2.10 VGA Controller

The SiS 5598 Chip with built-in VGA controller is a highly integrated single chip solution for Pentium PCI/ISA system. A portion of on-board DRAM is shared of maximum 4 Mbytes by the integrated VGA controller.

The SiS 5598 Chip consists of Host-to-PCI bridge function, PCI to ISA bridge function, PCI/IDE function, Universal Serial Bus host/hub function, Integrated RTC, Integrated Keyboard Controller and Graphics/Video accelerate function.

SiS 5598 Chip supports Enhanced Power Management, including legacy Power Management Unit and Advanced Configuration and Power Interface (ACPI). It also supports ATA Synchronous DMA transfer protocol to improve the IDE performance and Common Architecture for moving ISA function to PCI to improve system performance.

JP2 : VGA Enable Selection

PIN NO.	Address
*OFF	Enable
ON	Disable

*) : default setting

2.11 DiskOnChip? Address Setting

The HS-5210/5020 provides a U9 socket for install the DiskOnChip? module.

A JP7 may select the starting memory address of the DiskOnChip? (D.O.C.) for avoid the mapping area with any other memory devices. If you have another extra memory devices in the system with the same memory, neither the HS-5210/5020 nor the extra memory devices will function normally. Please setting both at different memory address mapping.

JP7 : DiskOnChip? Address

PIN NO.	Address
*1-2	D000
3-4	D800

*) : default setting

The D.O.C. function allows the system in using without FDD nor HDD. The D.O.C. may formatting as driver C: or driver A:. User may also easily uses the DOS's commands such as FORMAT, SYS, COPY, XCOPY, DISCOPY and DISKCOMP etc. This is means that the D.O.C. may uses as driver-A if the system without FDD-A for ambient application. Please contact with your supplier for different size D.O.C. module.

2.12 BIOS Type Selection

The HS-5210/5020 provides a JP5 for selects the type of flash chip in using as the BIOS. The manufacturer provides 29C010 on the board.

JP5 : BIOS Type Selection

PIN NO.	Address
1-2	29C010
*2-3	28F010

*) : default setting

Chapter-3

Connection

This chapter gives all necessary information of the peripheral's connections, switches and indicators.

3.1 The Floppy Disk Drive Connector

A standard 34-pin header daisy-chain driver connector provides as CN5 with following pin assignment. Total two FDD drivers may connect.

⌘ CN5 : FDD CONNECTOR

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GROUND	2	REDUCE WRITE
3	GROUND	4	N/C
5	GROUND	6	N/C
7	GROUND	8	INDEX#
9	GROUND	10	MOTOR ENABLE A#
11	GROUND	12	DRIVE SELECT B#
13	GROUND	14	DRIVE SELECT A#
15	GROUND	16	MOTOR ENABLE B#
17	GROUND	18	DIRECTION#
19	GROUND	20	STEP#
21	GROUND	22	WRITE DATA#
23	GROUND	24	WRITE DATA#
25	GROUND	26	TRACK 0#
27	GROUND	28	WRITE PROTECT#
29	GROUND	30	READ DATA#
31	GROUND	32	SIDE 1 SELECT
33	GROUND	34	DISK CHANGE#

3.2 PCI E-IDE Drive Connector

Two standard 40-pin header daisy-chain driver connectors provides as CN3 & CN4 with following pin assignment. Total four IDE (Integrated Device Electronics) drivers may connect.

CN3(IDE 1) : Primary IDE Connector

CN4(IDE 2) : Secondary IDE Connector

☞ CN3/CN4 : IDE Interface Connector

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	RESET	2	GROUND
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DATA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14
17	DATA 0	18	DATA 15
19	GROUND	20	N/C
21	N/C	22	GROUND
23	IOW#	24	GROUND
25	IOR#	26	GROUND
27	N/C	28	BALE - DEFAULT
29	N/C	30	GROUND# -DEFAULT
31	INTERRUPT	32	IOCS16#-DEFAULT
33	SA1	34	N/C
35	SA0	36	SA2
37	HDC CS0	38	HDC CS1#
39	HDD ACTIVE	40	GROUND

3.3 Parallel Port Connector

A standard 26-pin flat cable driver connector provides as CN2 with following pin assignment for connection to parallel printer.

☞ **CN2 : Parallel Port Connector**

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	STROBE	2	DATA 0
3	DATA 1	4	DATA 2
5	DATA 3	6	DATA 4
7	DATA 5	8	DATA 6
9	DATA 7	10	ACKNOWLEDGE
11	BUSY	12	PAPER EMPTY
13	PRINTER SELECT	14	AUTO FORM FEED
15	ERROR#	16	INITIALIZE
17	PRINTER SELECT LN#	18	GROUND
19	GROUND	20	GROUND
21	GROUND	22	GROUND
23	GROUND	24	GROUND
25	GROUND	26	GROUND

3.4 Serial Ports Connectors

The HS-5210/5020 offers two high speed NS16C550 compatible UARTs with Read/Receive 16 byte FIFO serial ports with one DB-9 external connector, and one internal 10-pin header connector.

☞ CN16 COM-1: Serial Port DB-9 Connector (HS-5210P/5020P only)

PIN NO.	DESCRIPTION
1	DATA CARRIER DETECT (DCD)
2	RECEIVE DATA (RXD)
3	TRANSMIT DATA (TXD)
4	DATA TERMINAL READY (DTR)
5	GROUND (GND)
6	DATA SET READY (DSR)
7	REQUEST TO SEND (RTS)
8	CLEAR TO SEND (CTS)
9	RING INDICATOR (RI)

☞ CN12 COM-2 / CN13 COM-1 : Serial Ports 10-pin Header

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	DCD	2	DSR
3	RXD	4	RTX
5	TXD	6	CTX
7	DTR	8	RI
9	GND	10	NC

3.5 Keyboard Connectors

The HS-5210/5020 offers two possibilities for keyboard connections to external PS/2 type keyboard at CN20, or an internal 5-pin header at CN1.

☞ **CN1 : 5-pin Header Keyboard Connector**

PIN NO.	DESCRIPTION
1	KEYBOARD CLOCK
2	KEYBOARD DATA
3	N/C
4	GROUND
5	+5V

☞ **CN20 : 6-pin Mini-DIN Keyboard Connector**

PIN NO.	DESCRIPTION
1	KEYBOARD DATA
2	N/C
3	GROUND
4	+5V
5	KEYBOARD CLOCK
6	N/C

3.6 Power's LED, Key-Lock and Reset Button

The following provides the pin information for Power's LED indicator, Key-Lock and Reset Button connections from CN8, CN7 and JP8.

☞ **CN7 : POWER LED & KEYLOCK**

PIN NO.	DESCRIPTION
1	POWER LED ANODE
2	NC
3	GROUND
4	KEYLOCK
5	GROUND

JP8 : RESET BUTTON

PIN NO.	DESCRIPTION
1	EXTERNAL RESET
2	GROUND

CN8 : HDD LED connector

PIN NO.	DESCRIPTION
1	HDD ACTIVE#
2	+5V

3.7 External Speaker

The HS-5210/5020 has an on-board buzzer. And it also provides the CN6 in allows user to connecting to the external speaker.

CN6 : Speaker Connector

PIN NO.	DESCRIPTION
1	SPEAKER SIGNAL
2	NC
3	GROUND
4	+5V

3.8 PS/2 Mouse 6-pin Mini-DIN Connector

The HS-5210/5020 provides an external PS/2 mouse connector at CN17 with following pin information.

CN17 : PS/2 Mouse Connector

PIN NO.	DESCRIPTION
1	DATA
2	NC
3	GROUND
4	+5V
5	CLK
6	NC

3.9 VGA Connectors

The HS-5210/5020 provides two possible connectives of VGA connections. One standard DB-15 external VGA connector as following CN14 pin information.

☞ **CN18 : 15-pin DB-15 Female VGA connector**

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	RED	2	GREEN
3	BLUE	4	NC
5	GROUND	6	GROUND
7	GROUND	8	GROUND
9	NC	10	GROUND
11	NC	12	NC
13	HSYNC	14	VSYNC
15	NC		

3.10 IR Connector

The HS-5210/5020 provides a 5-pin internal IR communication connector. The CN9 provides for IrDA 1.0 specification application.

☞ **CN9 : 5-PIN IR CONNECTOR**

PIN NO.	DESCRIPTION
1	Vcc
2	NC
3	IRRX
4	GROUND
5	IRTX

3.11 Extra Power Connector

The HS-5210/5020 provides an 8-pin extra DC power connector CN14 for internal power connection at a single board application. Please refer to the following table for detail pin information.

☞ **CN14 : 8P Extra Power Connector**

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	Vcc	2	+12V
3	-12V	4	GROUND
5	GROUND	6	-5V
7	+12V	8	Vcc

3.12 USB Ports Connector

The HS-5210/5020 provides two internal 4-pin USB ports connectors. Please refer to the following detail pin information.

☞ **CN10, CN11 : 4-pin Header USB connector**

PIN NO.	CN10(USB0)	PIN NO.	CN11(USB1)
1	Vcc	1	Vcc
2	BD0-	2	BD1-
3	BD0+	3	BD1+
4	GROUND	4	GROUND

3.13 Fast Ethernet Connector

The Fast Ethernet controller provides with 32-bit performance, PCI bus master capability, and full compliance with IEEE 802.3 10/100Based-T specifications.

For 10/100Base-T operation, please connect the network connection by plugging one end of the cable into the 9-pin RJ-45 CN13 Connector.

CN13 : Ethernet Connector (9-pin RJ-45)

PIN NO.	DESCRIPTION
1	TX+
2	TX-
3	RX+
4	NC
5	NC
6	RX-
7	NC
8	NC
9	Ground

For indication out the LAN operating status, the board provides three LED indicators in show out the status at follows:

- LD1: LED indicator lighting shows 10-Based data rating
- LD2: LED indicator lighting shows 100-Based data rating
- LD4: LED indicator lighting shows LAN in active

Chapter-4

AWARD BIOS Setup

The board uses Award PCI/ISA BIOS for the system configuration. The Award BIOS setup program is designed to provide the maximum flexibility in configuring the system by offering various options which could be selected for end-user requirements. This chapter is written to assist you in the proper usage of these features.

To access AWARD PCI/ISA BIOS Setup program, press key during memory testing when first power on. The Main Menu will be displayed at this time.

4.1 Main Menu

Once you enter the Award BIOS CMOS Setup Utility, the Main Menu will appear on the screen. The Main Menu allows you to select from several setup functions and two exit choices. Use the arrow keys to select among the items and press <Enter> to enter the sub-menu.

Note that a brief description of each highlighted selection appears at the bottom of the screen.

ROM PCI/ISA BIOS (xxxxxxxx)
CMOS SETUP UTILITY
AWARD SOFTWARE, INC.

STANDARD CMOS SETUP	INTEGRATED PERIPHERALS
BIOS FEATURES SETUP	SUPERVISOR PASSWORD
CHIPSET FEATURES SETUP	USER PASSWORD
POWER MANGEMENT SETUP	IDE HDD AUTO DETECTION
PCI CONFIGURATION SETUP	SAVE & EXIT SETUP
LOAD BIOS DEFAULTS	EXIT WITHOUT SAVING
LOAD SETUP DEFAULTS	
Esc : Quit	←←←← : Select Item
F10 : Save & Exit	(Shift)F2 : Change Color

4.2 Standard CMOS Setup

The Standard Setup is used for the basic hardware system configuration. The main function is for Data/Time and Floppy/Hard Disk Drive settings. Please refer to the following screen for the setup. When the IDE hard disk drive you are using is larger than 528MB, please set the HDD mode to **LBA** mode. Please use the IDE Setup Utility in BIOS SETUP to install the HDD correctly.

ROM PCI/ISA BIOS (xxxxxxxx)
STANDARD CMOS SETUP
AWARD SOFTWARE, INC.

Data (mm:dd:yy) : Tue, Oct. 19 1999								
Time (hh:mm:ss) : 00:00:00								
	TYPE	SIZE	CYLS	HEAD	PRECOMP	LANDZ	SECTOR	MODE
Primary Master	: AUTO	0M	0	0	0	0	0	AUTO
Primary Slave	? AUTO	0M	0	0	0	0	0	AUTO
Secretary Master	AUTO	0M	0	0	0	0	0	AUTO
Secretary Slave	AUTO	0M	0	0	0	0	0	AUTO
Drive A	: 1.44M , 3.5 in.							
Drive B	: None							
				Base	Memory	:	640K	
				Extended	Memory	:	14336K	
Vedio	: EGA/VGA							
				Other	Memory	:	384K	
Halt On	: All Errors							
				Total	Memory	:	15360K	
ESC : Quit			DEL/DEL/DEL : Select Item			PU/PD/ + / - : Modify		
F1 : Help			(Shift) F2: Change Color					

4.3 BIOS Features Setup

This section allows you to configure your system for the basic operation. You have the opportunity to select the system' s default speed, boot-up sequence, keyboard operation, shadowing and security.

ROM PCI/ISA BIOS (xxxxxxxx)
 BIOS FEATURES SETUP
 AWARD SOFTWARE, INC.

Virus Warning	: Disabled	Video BIOS	Shadow	: Enabled
CPU Internal Cache	: Enabled	C8000-CBFFF	Shadow	: Disabled
External Cache	: Enabled	CC000-CFFF	Shadow	: Disabled
Quick Power On Self Test	: Disabled	D0000-D3FFF	Shadow	: Disabled
Boot Sequence	: A,C,SCSI	D4000-D7FFF	Shadow	: Disabled
Swap Floppy Drive	: Disabled	D8000-DBFFF	Shadow	: Disabled
Boot Up Floppy Seek	: Enabled	DC000-DFFFF	Shadow	: Disabled
Boot Up NumLock Status	: On			
Boot Up System Speed	: High			
Gate A20 Option	: Fast			
Memory Parity Check	: Enabled			
Typematic Rate Setting	: Disabled			
Typematic Rate (Chars/Sec)	: 6			
Typematic Delay (Msec)	: 250			
Security Option	: Setup			
PCI/VGA Palette Snoop	: Disable d	ESC	: Quit	: Select Item
OS Select For DRAM > 64MB	: Non-OS2	F1	: Help	PU/PD/+/-: Modify
		F5	: Old Values	(Shift) F2 : Color
		G6	: Load BIOS Defaults	
		G7	: Load Setup Defaults	

4.4 Chipset Features Setup

This section allows you to configure the system based on the specific features of the installed chipset. This chipset manages bus speeds and the access to the system memory resources, such as DRAM and the external cache. It also coordinates the communications between the conventional ISA and PCI buses. It must be stated that these items should never be altered. The default settings have been chosen because they provide the best operating conditions for your system. You might consider and make any changes only if you discover that the data has been lost while using your system.

ROM PCI/ISA BIOS (xxxxxxxx)
 BIOS FEATURES SETUP
 AWARD SOFTWARE, INC.

Auto Configuration	: Enabled	CPU to PCI Burst Mem. WR	: Disabled
L2 (WB) Tag Bit Length	: 8bits	ISA Bus Clock Frequency	: PCICLK/4
SDRAM RAS-to-CAS Delay	: Enabled	System BIOS Cacheable	: Enabled
NA# Enable	: Enabled	Video BIOS Cacheable	: Enabled
Starting Point of Paging	: 1T	Memory Hole at 15M-16M	: Disabled
Refresh Cycle Time (us)	: 187.2	VGA Shared Memory Size	: 1MB
RAS Pulse Width Refresh	: 6T	VGA Memory Clock (MHz)	: 55
RAS Precharge Time	: 4T		
RAS to CAS Delay	: 4T		
CAS# Pulse Width (FP)	: 2T		
CAS# Pulse Width (EDO)	: 1T		
RAMW# Assertion Timing	: 3T		
CAS Precharge Time (FP)	: 1T/2T		
CAS Precharge Time (EDO)	: 1T/2T		
SDRAM Wait State Control	: 1WS	ESC : Quit	ESC ESC ESC : Select Item
Enhanced Memory Write	: Disabled	F1 : Help	PU/PD/+/-: Modify
Read Prefetch Memory RD	: Enabled	F5 : Old Values	(Shift) F2 : Color
CPU to PCI Post Write	: 3T	F6 : Load BIOS Defaults	
		F7 : Load Setup Defaults	

4.5 Integrated Peripherals

The IDE hard drive controllers can support up to two separate hard drives. These drives have a master/slave relationship which is determined by the cabling configuration used to attach them to the controller. Your system supports two IDE controllers--a primary and a secondary--so you can install up to four separate hard disks.

PIO means Programmed Input /Output. Rather than having the BIOS issue a series of commands to affect the transfer to or from the disk drive, PIO allows the BIOS to tell the controller what it wants and then let the controller and the CPU perform the complete task by them. This is much simpler and more efficient (also faster).

ROM PCI/ISA BIOS (xxxxxxxx)
 INTEGRATED PERIPHERALS
 AWARD SOFTWARE, INC.

IDE HDD Block Mode	: Both	USB Keyboard Support	: Disabled
IDE Primary Master PIO	: Auto	Power Button Over Ride	: Enabled
IDE Primary Slave PIO	: Auto	Ring Power Up Control	: Enabled
IDE Secretary Master PIO	: Auto	GPIO5 Power Up Control	: Enabled
IDE Secretary Slave PIO	: Auto	Power Up by Alarm	: Disabled
IDE Burst Mode	:		
IDE Data Port Post Write	: Enabled		
IDE HDD Block Mode	:		
Onboard FDD Controller	: Enabled		
Onboard Serial Port 1	: 3F8/IRQ4		
Onboard Serial Port 2	: 2F8/IRQ3		
UART 2 Mode	: Standard		
Onboard Parallel Port	: 378/IRQ7	ESC	: Quit
Onboard Parallel Mode	: SPP	F1	: Help
		F5	: Old Values
		F6	: Load BIOS Defaults
		F7	: Load Setup Defaults
USB Controller	: Enabled		
			↑ ↓ ← → : Select Item
			PU/PD/+/=: Modify
			(Shift) F2 : Color

4.6 Power Management Setup

The Power Management Setup allows user to configure the system for saving energy in a most effective way while operating in a manner consistent with his own style of computer use.

ROM PCI/ISA BIOS (xxxxxxxx)
 INTEGRATED PERIPHERALS
 AWARD SOFTWARE, INC.

Power Management	: Disabled	VGA Activity	: Disabled
PM Control by APM	: Yes	IRQ3 (COM2)	: Enabled
Video Off Method	: Susp, stby ->Off	IRQ4 (COM1)	: Enabled
Video Off After	: V/H SYNC + Blank	IRQ5 (LPT2)	: Enabled
Switch Function	: Break/Wake	IRQ6 (Floppy Dick)	: Enabled
Doze Speed (div by)	: 2	IRQ7 (LPT1)	: Enabled
Standby Speed (div by)	: 3	IRQ8 (RTC Alarm)	: Disabled
MODEM Use IRQ	: 3	IRQ9 (IRQ2 Redir)	: Enabled
Hot Key Power Off	: Disabled	IRQ10 (Reserved)	: Enabled
		IRQ11 (Reserved)	: Enabled
** PM Times **		IRQ12 (PS/2 Mouse)	: Enabled
HDD Off After	: Disabled	IRQ13 (Coprocesor)	: Enabled
Doze Mode	: Disabled	IRQ14 (Hard Disk)	: Enabled
Standby Mode	: Disabled	IRQ15 (Reserved)	: Enabled
Suspend Mode	: Disabled		
		ESC	: Quit <i>Esc Esc Esc</i> : Select Item
** PM Events **		F1	: Help PU/PD/+/-: Modify
COM Ports Activity	: Enabled	F5	: Old Values (Shift) F2 : Color
LPT Ports Activity	: Enabled	F6	: Load BIOS Defaults
HDD Ports Activity	: Enabled	F7	: Load Setup Defaults

Chapter-5

A Brief Browse of 10/100 based-T LAN RTL-8139's Installation Software

This chapter only provides for HS-5210/5020. The content herein is not for HS-5210P/5020P.

The on board provides one 32-bit PCI 10/100 based-T Ethernet LAN interface connection for easy using this Industrial Single Board in connection to-with Novell NE2000 compatible LAN network system.

The design is base on RTL 8139 chipset with, provides a 10/100 based-T NE2000 compatible interfaces. We here provide some information on the installation for your first reference.

The delivery of the software packages with HS-5210/5020 which including a easy access help manual by files from. Please read all following help manual first before your installation of this LAN system.

For completed information, please browse at
<http://www.realtek.com.tw>