AR-B1420
INDUSTRIAL GRADE
486DX CPU CARD
User's Guide

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0.PREFACE

0.1 COPYRIGHT NOTICE AND DISCLAIMER

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0.2 WELCOME TO THE AR-B1420 CPU BOARD

This guide introduces you to the Acrosser AR-B1420 CPU board.

This information describes this card's functions, features, and how to start, set up and operate your AR-B1420. You also can find general system information here.

0.3 BEFORE YOU USE THIS GUIDE

If you have not already installed this AR-B1420, refer to Chapter 3, "Setting Up The System" in this guide. Check the packing list. Make sure the accessories are complete.

The AR-B1420 diskette provides the newest information about the card**. Please refer to the README.DOC file of the enclosed utility diskette**. It contains the modification, hardware & software information, and it has updates to product functions that may not be mentioned here.

0.4 RETURNING YOUR BOARD FOR SERVICE

If your board requires servicing, contact the dealer from whom you purchased the product for service information. If you need to ship your board to us for service, be sure it is packed in a protective carton. We recommend that you keep the original packaging for this purpose.

You can assure efficient servicing of your product by following these guidelines:

- Include your name, address, daytime telephone and facsimile numbers and E-mail.
- A description of the system configuration and/or software at the time is malfunction,
- And a brief description of the symptoms.

0.5 TECHNICAL SUPPORT AND USER COMMENTS

User's comments are always welcome as they assist us in improving the usefulness of our products and the understanding of our publications. They form a very important part of the input used for product enhancement and revision.

We may use and distribute any of the information you supply in any way we believe appropriate without incurring any obligation. You may, of course, continue to use the information you supply.

If you have suggestions for improving particular sections or if you find any errors, please indicate the manual title and book number.

Please send your comments to Acrosser Technology Co., Ltd. or your local sales representative.

Internet electronic mail to: **webmaster@acrosser.com**

Check our FAQ sheet for quick fixes to known technical problems.

0.6 ORGANIZATION

This manual covers the following topics (see the Table of Contents for a detailed listing):

- Chapter 1, "Overview", provides an overview of the system features and packing list.
- Chapter 2, "System Controller" describes the major structure.
- Chapter 3, "Setting Up the System", describes how to adjust the jumper, and the connector settings.
- Chapter 4, "System Installation", describes setup procedures and the utility diskette.
- Chapter 5, "Solid State Disk", describes the S.S.D and D.O.C Installation
- Chapter 6, "BIOS Console", provides the BIOS settings and explanations.
- Chapter 7, "Specifications"
- Chapter 8, "Placement & Dimensions"
- Chapter 9, "Programming RS-485"
- Chapter 10 "Index"

0.7 STATIC ELECTRICITY PRECAUTIONS

Before removing the board from its anti-static bag, read this section about static electricity precautions.
Static electricity is a constant danger to computer systems. The charge that can build up in your body may be more than sufficient to damage integrated circuits on any PC board. It is, therefore, important to observe basic precautions whenever you use or handle computer components. Although areas with humid climates are much less prone to static build-up, it is always best to safeguard against accidents that may result in expensive repairs. The following measures should generally be sufficient to protect your equipment from static discharge:

- Touch a grounded metal object to discharge the static electricity in your body (or ideally, wear a grounded wrist strap).
- When unpacking and handling the board or other system components, place all materials on an anti static surface.
- Be careful not to touch the components on the board.

1. OVERVIEW

This chapter provides an overview of your system features and capabilities. The following topics are covered:

- Introduction
- Packing List
- Features

1.1 INTRODUCTION

The AR-B1420 is an all-in-one 486 (PC/104) industrial grade CPU module that has been designed to withstand continuous operation in harsh environments. This board can stand alone as a CPU card or be used with other PC/104 compatible cards. The total on-board memory for the AR-B1420 can be configured from 8MB to 144MB by using any 144-pin type SoDIMM.

The 8 layer PCB CPU card is equipped with an IDE HDD interface, a floppy disk drive adapter, 1 parallel port, 2 serial ports and a watchdog timer. Its dimensions are as compact as 90.2mm X 95.9mm. Its highly condensed features make it an ideal cost/performance solution for high-end commercial and industrial applications where CPU speed and mean time between failures is critical.

The AR-B1420 provides 1 bus interface: a PC/104 compatible expansion bus, which can be turned into an ISA bus with the addition of an adapter. Based on the PC/104 expansion bus, you could easily install thousands of PC/104 modules from hundreds of venders around the world. You can also directly connect the power supply to the AR-B1420 on-board power connector in standalone applications.

A watchdog timer, which has a software programmable time-out interval, is also provided on this CPU card. It ensures that the system does not hang-up if a program can not execute normally.

A super I/O chip (W83977) is embedded in the AR-B1420 card. It combines the functions of a floppy disk drive adapter, two serial (with 16C550 UART) adapters and 1 parallel adapter in one chip. The I/O port configurations can be set up in BIOS setup program.

As a UART, the chip supports serial to parallel conversions on data characters received from a peripheral device or a MODEM, and parallel to serial conversions on data character received from the CPU. The UART includes a programmable baud rate generator, and a processor interrupt system. As a parallel port, the W83977 provides the user with a fully bi-directional parallel centronics-type printer interface.

The VGA controller also supports CRT color monitors. It can be connected to create a compact video solution for the industrial environment.

1.2 PACKING LIST

These accessories are included with the system. Before you begin installing your AR-B1420 board, take a moment to make sure that the following items have been included inside the AR-B1420 package:

- The quick setup guide
- 1 AR-B1420 CPU card
- 1 Hard disk drive interface cable (2.0 mm pin pitch)
- 1 Floppy disk drive interface cable(2.54 mm pin pitch)
- 1 4-in-1 adapter cable for COM1/COM2, parallel, and VGA
- 1 keyboard/ PS/2 mouse adapter cable
- 1 Software utility diskette
- 1 power cable
- 1 kit of screws

1.3 FEATURES

This system provides a number of special features that enhance its reliability, ensure its availability, and improve its expansion capabilities, as well as its hardware structure.

- All-In-One designed 486DX CPU card (Intel 486 DX grade)
- Supports ST STPC Client 66/75/120 MHz (onboard 66 MHz CPU as the standard model)
- Supports PC/104 bus.
- Supports 1 SoDIMM type DRAM for 8 MB to 64 MB EDO RAM
- Supports D.O.C. up to 144MB.
- Licensed AMI BIOS.
- IDE hard disk drive interface.
- Floppy disk drive interface.
- Bi-direction parallel interface.
- 2 serial ports with 16C550 UART.
- Programmable watchdog timer.
- Supports 4 TTL inputs and 4 TTL outputs
- 8 layer PCB.

2. SYSTEM CONTROLLER

This chapter describes the major structure of the AR-B1420 CPU board. The AR-B1420 is mainly composed of a Single PC ChipSet and a Peripheral Chipset. A functional block diagram follows.

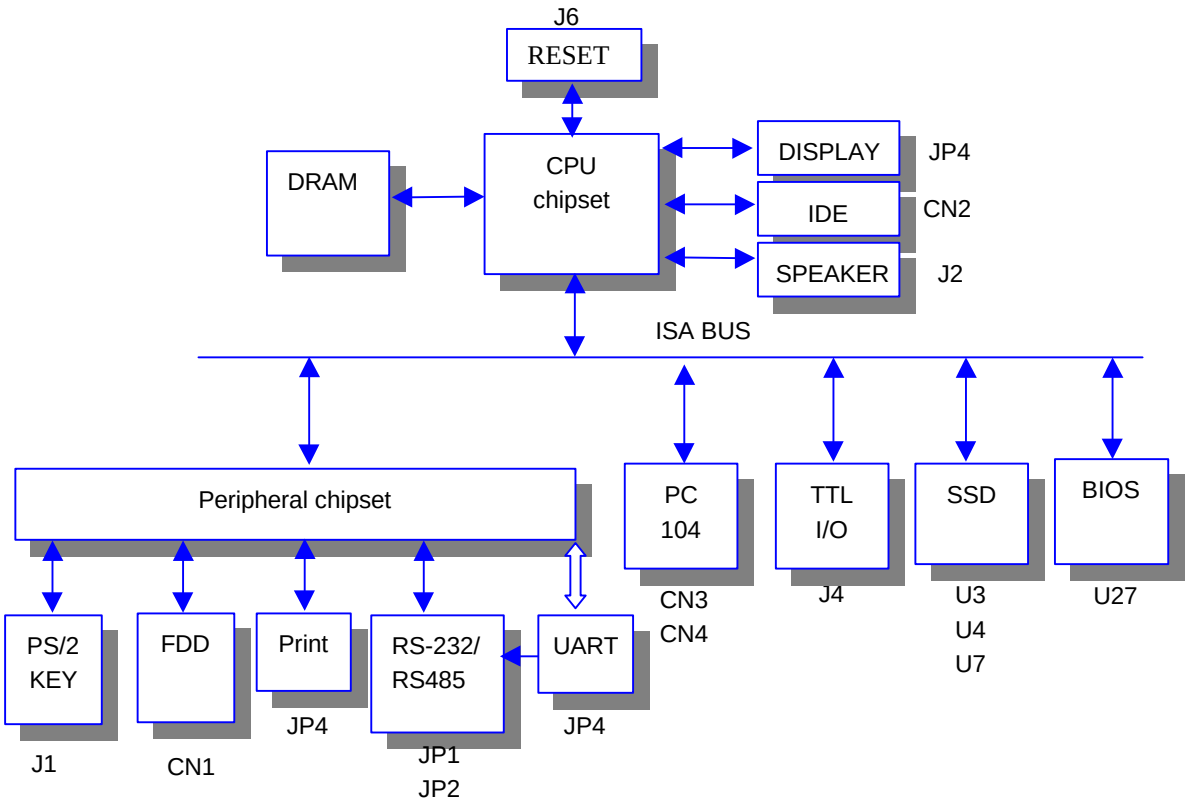


Figure 2-1 System Block Diagram

2.1 SINGLE PC CHIPSET

The single PC Chipset integrates a fully static X86 processor, which is fully compatible with X86 processors and combines with a powerful chipset, graphics and video pipelines to provide a PC compatible subsystem on a single device. The performance of the device is comparable with the performance of a typical P5 generation system. This device is packaged in a 388 Ball Grid Array (PBGA). At the heart of the Single PC Chipset is an advanced 64-bit processor block, dubbed the 5ST86. The 5ST86 includes a powerful X86 processor core along with a 64-bit DRAM controller, advanced 64-bit accelerated graphics and video controller, a high speed PCI local-bus controller and industry standard PC chip set functions (interrupt controller, DMA controller, interval timer and ISA bus) and an EIDE controller.

The single PC Chipset makes use of a tightly coupled Unified Memory Architecture (UMA), where the same memory array is used for CPU main memory and graphics frame-buffer. This means a reduction in total system memory for system performances that are equal to that of a comparable frame buffer and system memory based system. System performance is also generally improved, due to the higher memory bandwidth allowed by attaching the graphics engine directly to 64-bit processor host interface running at the speed of the processor bus rather than the traditional PCI bus. Graphics functions are controller through the on chip graphics engine and the monitor display is produced through the 2D graphics display engine. The graphics resolution supported is a maximum of 1280X1024 at a 75Hz refresh rate and is VGA and SVGA compatible. Horizontal timing fields are VGA compatible while the vertical fields are extended by one bit to accommodate the above display resolution. The frame buffer can occupy a space anywhere in the first four Mbytes of physical main memory.

The 64-bit wide memory array provides the system with 200Mb/s bandwidth, double that of an equivalent 32-bit system. This allows for higher resolution screens and greater color depth.

The standard PC chipset functions (DMA, Interrupt controller, timers, power management logic) are integrated

together with the X86 processor core. Additional functions are accessed by the single PC Chipset via the ISA bus. An EIDE port is provided for storage devices such as hard disks and CD-ROMs, bridging directly to the PCI bus.

2.2 PERIPHERAL CHIPSET

The peripheral Chipset on AR-B1420 integrates the disk driver adapter, serial port (UART), parallel port configurable plug-and-play registers in one chip, plus additional features: ACPI,8042 keyboard controller with PS/2 mouse support , Real Time Clock,14 general purpose I/O ports, and full 16-bit address decoding.
The disk driver adapter functions include a floppy disk driver controller compatible with the industry standard 82077/765, a data separator, a write pre-compensation circuit, decode logic, data rate selection, a clock generator, driver interface control logic, and interrupt/ DMA logic. The wide range of functions are integrated onto one chip greatly reduces the number of components required for interfacing with floppy disk drivers. This disk driver adapter supports up to four 360K, 720K, 1.2M, 1.44M, or 2.88M disk drives and data transfer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s, 1Mb/s, and 2 Mb/s.

The Peripheral Chipset provides two high-speed serial communication ports (UARTs), one of which supports serial infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupt system. Both UARTs provide legacy speed with baud rate 115.2K and provide advanced speed with baud rates of 230k, 460k, and 921k bps which support higher speed modems. In addition, on the AR-B1420 board dual RS-485 ports are offered.

The Peripheral Chipset supports one PC–Compatible printer port (SPP), Bi-directional printer port (BPP) and also Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP).

The configuration registers support mode selection, function enable/disable, and power down function selection. Furthermore, the configurable PnP features are compatible with the Windows 95 ™plug-and-play, which makes system resource allocation more efficient than ever.

The keyboard controller is based on an 8042 compatible instruction set with a 2K Byte programmable ROM and a 256-Byte RAM bank. Keyboard BIOS firmware is available with optional AMIKEY-2, Phoenix MultiKey/42, or customer code.

The Peripheral Chipset provides a set of flexible I/O control functions to system designer through a set of general purpose I/O ports. These GPIO ports may serve as simple I/O or may individually be configured to provide a pre-defined alternate function. The Peripheral Chipset is made to fully comply with the Microsoft ™PC97 Hardware Design Guide and IRQs, DMAs, I/O space resources are flexible to meet ISA PnP requirements.

2.3 DMA CONTROLLER

The equivalent of two 8237AT compatible DMA controllers built into the Single PC Chipset are implemented on the AR-B1420 board. Each controller is a four-channel DMA device that will generate the memory addresses and control signals necessary to transfer information directly between a peripheral device and memory. This allows high-speed information transfer with less CPU intervention. The two DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1) and three channels for transfers to 16-bit peripherals (DMA2). DMA2 channel 0 provides the cascade interconnection between the two DMA devices, thereby maintaining IBM PC/AT compatibility.

The Following is the system information for the DMA channels:

Slave with four 8-bit chnls	Master with three 16-bit chnls
DMA Controller 1	**DMA Controller 2**
Channel 0: Spare	Channel 4(0): Cascade for controller 1
Channel 1: IBM SDLC	Channel 5(1): Spare
Channel 2: Diskette adapter	Channel 6(2): Spare
Channel 3: Spare	Channel 7(3): Spare

Table 2-1 DMA Channel Controller

2.4 KEYBOARD CONTROLLER

The KBC circuit of the peripheral chipset is designed to provide the functions needed to interface a CPU with a keyboard and/or a PS/2 mouse, and can be used with IBM®-compatible personal computers orPS/2-based systems. The controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. Then, the controller will assert an interrupt to the system when data is placed in its output buffer. The keyboard and PS/2 mouse are required to acknowledge all data transmissions. No transmission should be sent to the keyboard or PS/2 mouse until an acknowledge is received for the previous data byte.

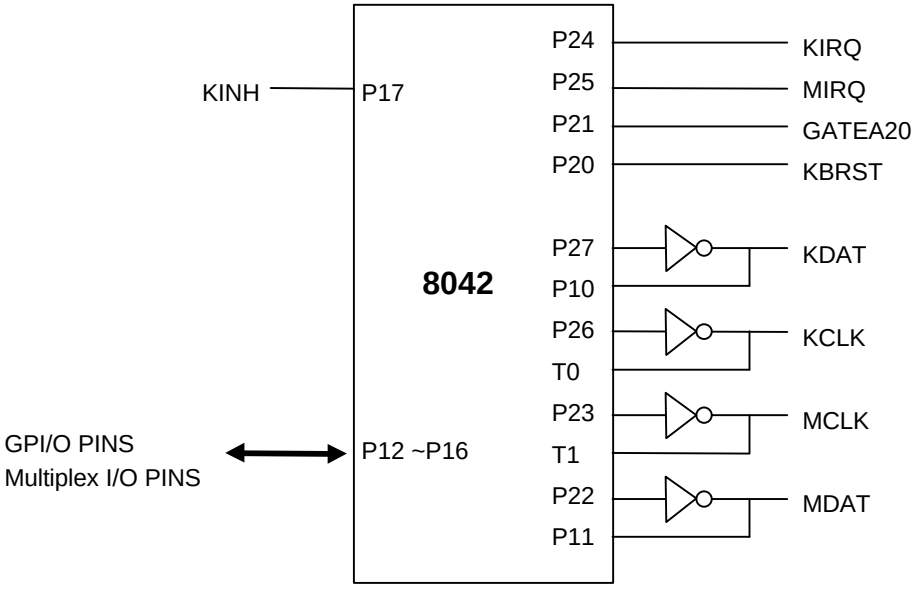


Figure 2-2 Keyboard and Mouse Interface

2.5 INTERRUPT CONTROLLER

The equivalent of two 8259 Programmable Interrupt Controllers (PIC) are included on the AR-B1420 board. They accept requests from peripherals, resolve priorities on pending interrupts in service, issue interrupt requests to the CPU, and provide vectors which are used as acceptance indices by the CPU to determine which interrupt service routine to execute. These two controllers are cascaded with the second controller representing IRQ8 to IRQ15, which is rerouted through IRQ2 on the first controller.

The following is the system information of interrupt levels:

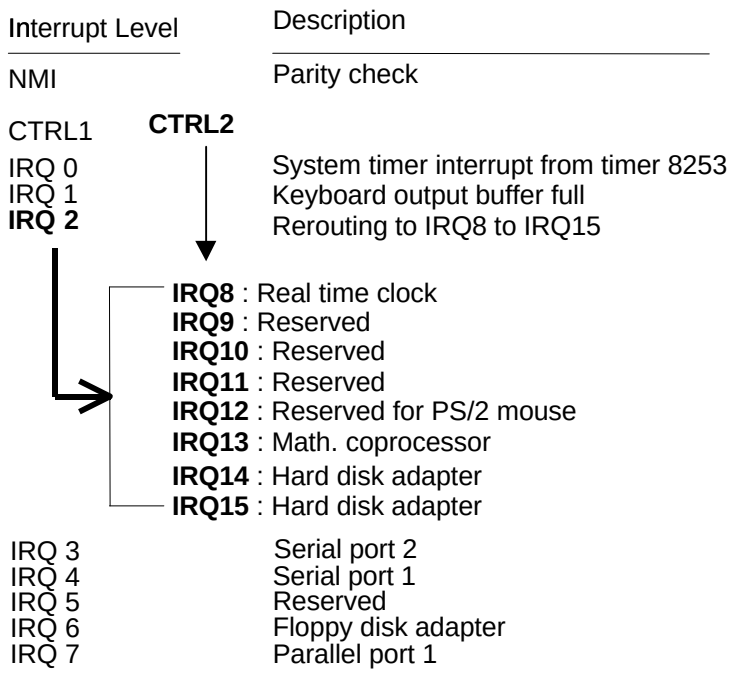


Figure 2-3 Interrupt Controller

Note: IRQ14 and IRQ15 are configured for the Hard Disk adapter only and can not be used for other devices.

2.6 I/O PORT ADDRESS MAP

Hex Range	Device
000-01F	DMA controller 1
020-021	Interrupt controller 1
022-023	STPC Client Address
040-04F	Timer 1
050-05F	Timer 2
060-06F	8042 keyboard/controller
070-071	Real-time clock (RTC), non-maskable interrupt (NMI)
080-09F	DMA page registers
0A0-0A1	Interrupt controller 2
0C0-0DF	DMA controller 2
0F0	Clear Math Co-processor
0F1	Reset Math Co-processor
0F8-0FF	Math Co-processor
170-178	Fixed disk 1
1F0-1F8	Fixed disk 0
201	Game port
208-20A	EMS register 0
218-21A	EMS register 1
278-27F	Parallel printer port 2 (LPT 2)
2E8-2EF	Serial port 4 (COM 4)
2F8-2FF	Serial port 2 (COM 2)
300-31F	Prototype card/streaming type adapter
320-33F	LAN adapter
378-37F	Parallel printer port 1 (LPT 1)
380-38F	SDLC, bisynchronous
3A0-3AF	Bisynchronous
3B0-3BF	Monochrome display and printer port 3 (LPT 3)
3C0-3CF	EGA/VGA adapter
3D0-3DF	Color/graphics monitor adapter
3E8-3EF	Serial port 3 (COM 3)
3F0-3F7	Diskette controller
3F8-3FF	Serial port 1 (COM 1)
210-211	SSD IO port
216-217	TTL IO port

Table 2-2 I/O Port Address Map

2.7 MEMORY SPACE

Memory Map	Assignment
0000000-009FFFF	System Memory Used by DOS and Application
00A0000-00BFFFF	Display Buffer Memory for VGA/ EGA/ CGA/ MONOCHROME adapter
00C0000-00DFFFF	Reserved for I/O Device BIOS ROM or RAM Buffer
00E0000-00EFFFF	Reserved for PCI Device ROM
00F0000-00FFFFF	System BIOS ROM
0100000-FFFFFFF	System Extension Memory

Table 2-3 Memory Space

Note 1: You can set up the S.S.D. data bank at either "C8000~CA000" or "D0000~D2000" by means of manual switch SW1 "Switch 3." Refer to Chapter 5 Solid State Disk.

Note 2: When the system uses D.O.C. flash memory, the hardware "SW1 Switch 4" should be set to "ON." Simultaneously, this setup will occupy extra 8K-memory size. Also Refer to Chapter 5 Solid State Disk. The following table exhibits the SW1 switch setup.

Note 3: If you have installed EMM386.EXE driver, please use the "X" option to prevent EMM386.EXE from using a particular range of segment address, which is used by AR-B1420, for an EMS page. For example, the line in CONFIG.SYS file write as: (if the memory configuration of AR-B1420 is C800:0)

DEVICE=C:\DOS\EMM386.EXE x=C800-C9FF

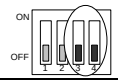
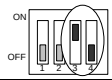
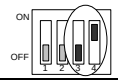
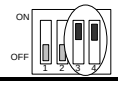
SW1	Memory	Memory Map	Extra Memory Size
Switch 3 set to "OFF" Switch 4 set to "OFF" 	S.S.D Data Bank	C8000~CA000	8K
Switch 3 set to "ON" Switch 4 set to "OFF" 	S.S.D Data Bank	D0000~D2000	8K
Switch 3 set to "OFF" Switch4 set to "ON" 	S.S.D Data Bank	C8000~CA000	8K
	D.O.C Data Bank	CA000~CC000	8K
Switch 3 set to "ON" Switch4 set to "ON" 	S.S.D Data Bank	D0000~D2000	8K
	D.O.C. Data Bank	D2000~D4000	8K

Table 2-4 SW1 Switch Setup

2.8 REAL-TIME CLOCK AND NON-VOLATILE RAM

The RTC with 242 bytes of RAM is a low-power device that provides a time-of-day clock in various formats and a calendar with century register. It has 2 alarms.

ADDRESS	REGISTER TYPE	REGISTER FUNCTION
00h	R/W	Register 00h: Seconds
01h	R/W	Register 01h: Seconds Alarm A
02h	R/W	Register 02h: Minutes
03h	R/W	Register 03h: Minutes Alarm A
04h	R/W	Register 04h: Hours
05h	R/W	Register 05h: Hours Alarm A
06h	R/W	Register 06h: Day of Week
07h	R/W	Register 07h: Date of Month
08h	R/W	Register 08h: Month
09h	R/W	Register 09h: Year
0Ah	R/W	Register 0Ah: Control Register
0Bh	R/W	Register 0Bh: Control Register (Bit 0 is Read Only)
0Ch	R	Register 0Ch: Status Register
0Dh	R	Register 0Dh: Status Register
0Eh-7Fh	R/W	Register 0Eh-7Fh: USER RAM

Table 2-5 Real Time Clock Address Map Bank

ADDRESS	REGISTER TYPE	REGISTER FUNCTION
00h-7Fh	R/W	Register 0h-7fh

Table 2-6 Real Time Clock Address Map Bank 1

2.9 TIMER

The AR-B1420 provides three programmable timers, each with a timing frequency of 1.19 MHz.

Timer 0 The output of this timer is tied to interrupt request 0. (IRQ 0)

Timer 1 This timer is used to trigger memory refresh cycles.

Timer 2 This timer provides the speaker tone.
Application programs can load different counts into this timer to generate various sound frequencies.

2.10 SERIAL PORT

2.10.1 Universal Asynchronous Receiver/Transmitter(UART A, UART B)

The UARTs are used to convert parallel data into serial format on the transmit side and convert serial data to parallel format on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and half (five-bit format only) or two stop bits. The UARTs are capable of handling divisors of 1 to 65535 and producing a 16x clock for driving the internal transmitter logic. Provisions are also included to use this 16x clock to drive the receiver logic. The UARTs also support the MIDI data rate. Furthermore, the UARTs also include complete modem control capability and a processor interrupt system that may be software trailed to the computing time required to handle the communication link. The UARTs have a FIFO mode to reduce the number of interrupts presented to the CPU. In each UART, there are 16-byte FIFOs for both receive and transmit mode..

The following table is summary of each ACE accessible register

DLAB	Port Address	Register
0	base + 0	Receiver buffer (read)
		Transmitter holding register (write)
0	base + 1	Interrupt enable
X	base + 2	Interrupt identification (read only)
X	base + 3	Line control
X	base + 4	MODEM control
X	base + 5	Line status
X	base + 6	MODEM status
X	base + 7	Scratched register
1	base + 0	Divisor latch (least significant byte)
1	base + 1	Divisor latch (most significant byte)

Table 2-7 ACE Accessible Registers

(1) Receiver Buffer Register (RBR)

Bit 0-7: Received data byte (Read Only)

(2) Transmitter Holding Register (THR)

Bit 0-7: Transmitter holding data byte (Write Only)

(3) Interrupt Enable Register (IER)

Bit 0: Enable Received Data Available Interrupt (ERBFI)
Bit 1: Enable Transmitter Holding Empty Interrupt (ETBEI)
Bit 2: Enable Receiver Line Status Interrupt (ELSI)
Bit 3: Enable MODEM Status Interrupt (EDSSI)
Bit 4: Must be 0
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(4) Interrupt Identification Register (IIR)

Bit 0: "0" if Interrupt Pending
Bit 1: Interrupt ID Bit 0
Bit 2: Interrupt ID Bit 1
Bit 3: Must be 0
Bit 4: Must be 0
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(5) Line Control Register (LCR)

Bit 0: Word Length Select Bit 0 (WLS0)
Bit 1: Word Length Select Bit 1 (WLS1)

WLS1	WLS0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: Number of Stop Bit (STB)
Bit 3: Parity Enable (PEN)
Bit 4: Even Parity Select (EPS)
Bit 5: Stick Parity
Bit 6: Set Break
Bit 7: Divisor Latch Access Bit (DLAB)

(6) MODEM Control Register (MCR)

Bit 0: Data Terminal Ready (DTR)
Bit 1: Request to Send (RTS)
Bit 2: Out 1 (OUT 1)
Bit 3: Out 2 (OUT 2)
Bit 4: Loop
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(7) Line Status Register (LSR)

Bit 0: Data Ready (DR)
Bit 1: Overrun Error (OR)
Bit 2: Parity Error (PE)
Bit 3: Framing Error (FE)
Bit 4: Break Interrupt (BI)
Bit 5: Transmitter Holding Register Empty (THRE)
Bit 6: Transmitter Shift Register Empty (TSRE)
Bit 7: Must be 0

(8) MODEM Status Register (MSR)

Bit 0: Delta Clear to Send (DCTS)
Bit 1: Delta Data Set Ready (DDSR)
Bit 2: Training Edge Ring Indicator (TERI)
Bit 3: Delta Receive Line Signal Detect (DSLSD)
Bit 4: Clear to Send (CTS)
Bit 5: Data Set Ready (DSR)
Bit 6: Ring Indicator (RI)
Bit 7: Received Line Signal Detect (RSLD)

(9) Divisor Latch (LS, MS)

	LS	MS
Bit 0:	Bit 0	Bit 8
Bit 1:	Bit 1	Bit 9
Bit 2:	Bit 2	Bit 10
Bit 3:	Bit 3	Bit 11
Bit 4:	Bit 4	Bit 12
Bit 5:	Bit 5	Bit 13
Bit 6:	Bit 6	Bit 14
Bit 7:	Bit 7	Bit 15

Desired Baud Rate	Divisor Used to Generate 16x Clock
300	384
600	192
1200	96
1800	64
2400	48
3600	32
4800	24
9600	12
14400	8
19200	6
28800	4
38400	3
57600	2
115200	1

Table 2-8 Serial Port Divisor Latch

2.11 PARALLEL PORT

(1) Register Address

Port Address	Read/Write	Register
base + 0	Write	Output data
base + 0	Read	Input data
base + 1	Read	Printer status buffer
base + 2	Write	Printer control latch

Table 2-9 Registers' Address

(2) Printer Interface Logic

The parallel portion of the W83977 makes the attachment of various devices that accept eight bits of parallel data at standard TTL level.

(3) Data Swapper

The system microprocessor can read the contents of the printer's Data Latch through the Data Swapper by reading the Data Swapper address.

(4) Printer Status Buffer

The system microprocessor can read the printer status by reading the address of the Printer Status Buffer. The bit definitions are described as follows:

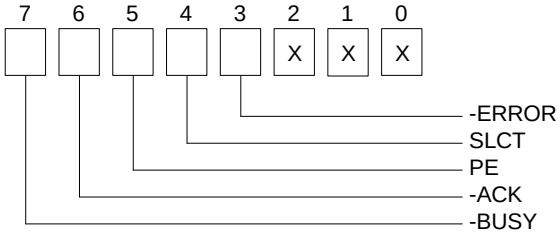


Figure 2-4 Printer Status Buffer

NOTE: X represents not used.

Bit 7: This signal may become active during data entry, when the printer is off-line during printing, or when the print head is changing position or in an error state. When Bit 7 is active, the printer is busy and can not accept data.

Bit 6: This bit represents the current state of the printer's ACK signal. A 0 means the printer has received the character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before receiving a BUSY message stops.

Bit 5: A 1 means the printer has detected the end of the paper.

Bit 4: A 1 means the printer is selected.

Bit 3: A 0 means the printer has encountered an error condition.

(5) Printer Control Latch & Printer Control Swapper

The system microprocessor can read the contents of the printer control latch by reading the address of printer control swapper. Bit definitions are as follows:

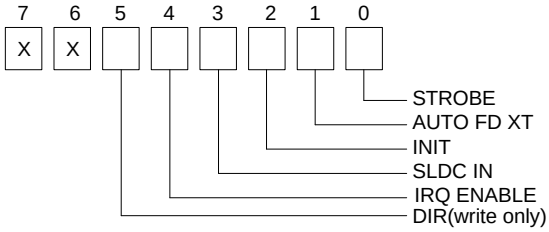


Figure 2-5 Bit's Definition

NOTE: X represents not used.

Bit 5: Direction control bit. When logic 1, the output buffers in the parallel port are disabled allowing data driven from external sources to be read; when logic 0, they work as a printer port. This bit is write only.

Bit 4: A 1 in this position allows an interrupt to occur when ACK changes from low state to high state.

Bit 3: A 1 in this bit position selects the printer.

Bit 2: A 0 starts the printer (50 microseconds pulse, minimum).

Bit 1: A 1 causes the printer to line-feed after a line is printed.

Bit 0: A 0.5 microsecond minimum highly active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.

3. SETTING UP THE SYSTEM

This section describes pin assignments for the system's external connectors and the jumper settings.

- Overview
- System Settings

3.1 OVERVIEW

The AR-B1420 is a PC/104 industrial grade CPU card that has been designed to withstand continuous operation in harsh environments. This section provides the hardware's jumper settings, the connectors' locations, and the pin assignments.

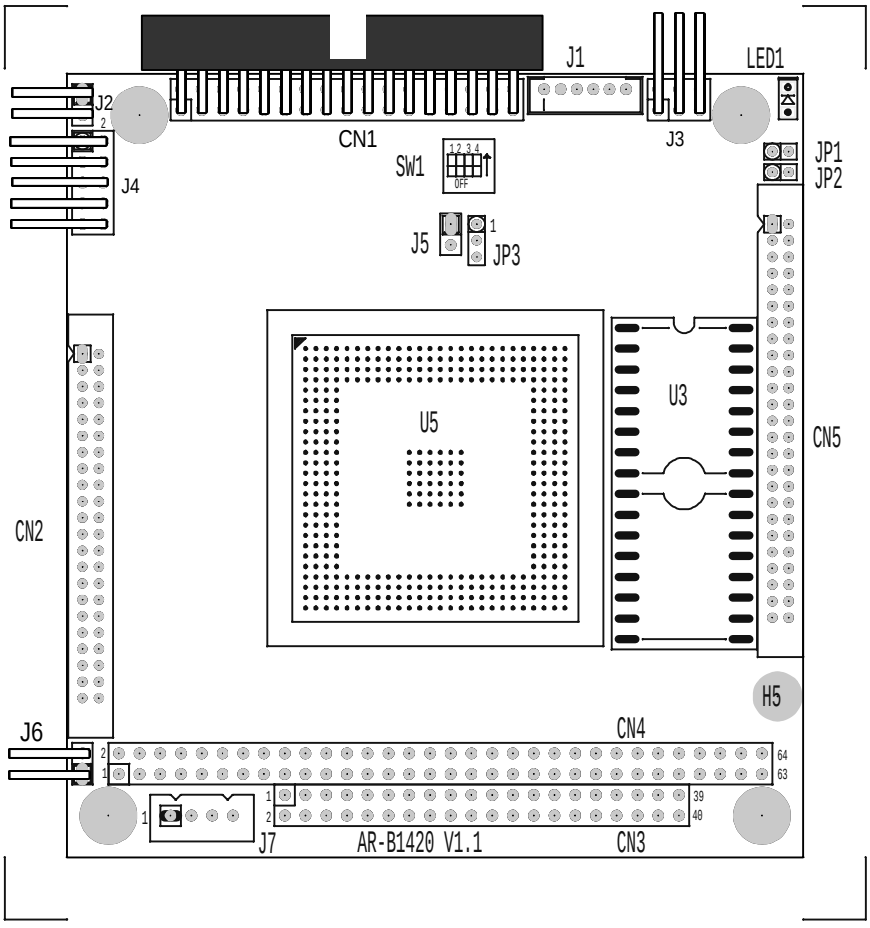


Figure 3-1 AR-B1420 Jumpers & Connectors Placement

3.2 SYSTEM SETTINGS

Jumper pins allow you to set specific system parameters. Set them by changing the pin location of the jumper blocks. (A jumper block is a small plastic-encased conductor that slips over the pins.) To change a jumper setting, remove the jumper from its current location with your fingers or small needle-nosed pliers. Place the jumper over the two pins designated for the desired setting. Press the jumper evenly onto the pins. Be careful not to bend the pins.

We will show the locations of the AR-B1420 jumper pins, and the factory-default settings in section 3.2.

CAUTION: Do not touch any electronic component unless you are safely grounded. Wear a grounded wrist strap or touch an exposed metal part of the system unit chassis. The static discharges from your fingers can permanently damage electronic components.

3.2.1 FDD Port Connector (CN1)

The AR-B1420 provides a 34-pin header type connector for supporting up to two floppy disk drives. To enable or disable the floppy disk controller, please use the BIOS Setup program.

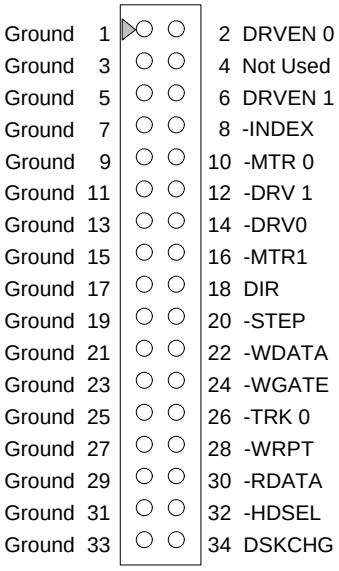


Figure 3-2 CN1: FDD Port connector

3.2.2 Hard Disk (IDE) Connector(CN2)

A 44-pin header type connector (CN2) is provided to interface with up to two embedded hard disk drives (IDE AT bus). This interface, through a 44-pin cable, allows the user to connect up to two drives in a "daisy chain" fashion. To enable or disable the hard disk controller, please use the BIOS Setup program. The following table illustrates the pin assignments of the hard disk drive's 44-pin connector.

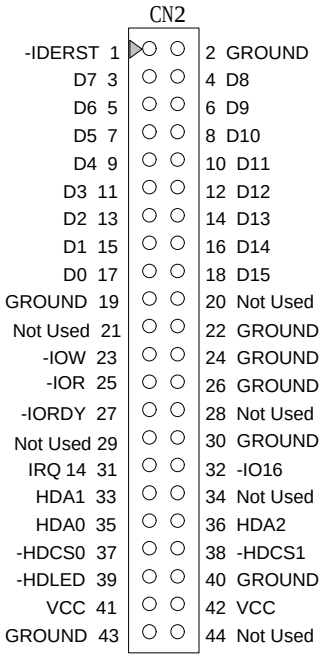


Figure 3-3 CN2: Hard Disk (IDE) Connector

3.2.3 Multi-function Port Connector (CN5)

CN5 integrates COM1/ COM2, the Parallel (Printer) port, and the VGA port into a single 50-pin connector. Pin1 to Pin10 are COM1 signals. Pin11 to Pin 20 are COM2 signals. Pin21 to Pin 40 are Parallel port signals. Pin41 to Pin 50 are VGA port signals. To use it, a 4-IN-1 adapter cable has to be connected to the CN5 (50-pin header type) connector. This adapter is included in your AR-B1420 package.

The AR-B1420 supports CRT color monitors. For different VGA display modes, your monitor must possess certain characteristics (different drivers for different modes) to display the mode you want.

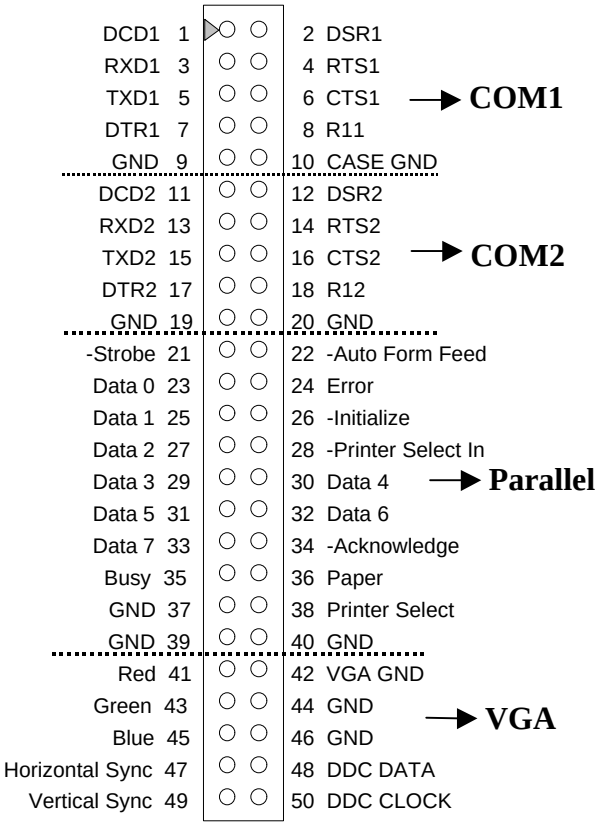


Figure 3-4 CN5: Multi-function Port Connector

3.2.4 PC/104 Connector

(1) 64 Pin PC/104 Connector Bus A & B (CN4)

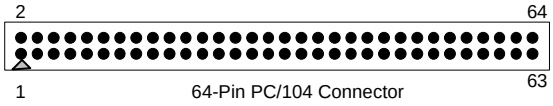


Figure 3-5 CN4: 64 Pin PC/104 Connector Bus A & B

CN4

	1	2	
-IOCHCK ---	A1	B1	--- GND
SD7 ---	A2	B2	--- RSTDRV
SD6 ---	A3	B3	--- +5 VDC
SD5 ---	A4	B4	--- IRQ9
SD4 ---	A5	B5	--- -5 VDC
SD3 ---	A6	B6	--- DRQ2
SD2 ---	A7	B7	--- -12 VDC
SD1 ---	A8	B8	--- -ZWS
SD0 ---	A9	B9	--- +12 VDC
-IOCHRDY---	A10	B10	--- GND
AEN ---	A11	B11	--- -SMEMW
SA19 ---	A12	B12	--- -SMEMR
SA18 ---	A13	B13	--- -IOW
SA17 ---	A14	B14	--- -IOR
SA16 ---	A15	B15	--- -DACK3
SA15 ---	A16	B16	--- DRQ3
SA14 ---	A17	B17	--- -DACK1
SA13 ---	A18	B18	--- DRQ1
SA12 ---	A19	B19	--- -REFRESH
SA11 ---	A20	B20	--- BUSCLK
SA10 ---	A21	B21	--- IRQ7
SA9 ---	A22	B22	--- IRQ6
SA8 ---	A23	B23	--- IRQ5
SA7 ---	A24	B24	--- IRQ4
SA6 ---	A25	B25	--- IRQ3
SA5 ---	A26	B26	--- -DACK2
SA4 ---	A27	B27	--- TC
SA3 ---	A28	B28	--- BALE
SA2 ---	A29	B29	--- +5 VDC
SA1 ---	A30	B30	--- OSC
SA0 ---	A31	B31	--- GND
GND ---	A32	B32	--- GND

Figure 3-6 CN4: 64-Pin PC/104 Connector Bus A & B Signal

(2) 40 Pin PC/104 Connector Bus C & D (CN3)

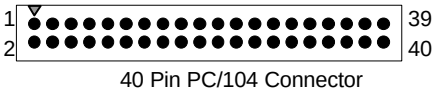


Figure 3-7 CN3: 40 Pin PC/104 Connector Bus C & D

CN3

	1	2	
GND ---	C1	D1	--- GND
-SBHE ---	C2	D2	--- -MEM16
LA23 ---	C3	D3	--- -IOCS16
LA22 ---	C4	D4	--- IRQ10
LA21 ---	C5	D5	--- IRQ11
LA20 ---	C6	D6	--- IRQ12
LA19 ---	C7	D7	--- IRQ15
LA18 ---	C8	D8	--- IRQ14
LA17 ---	C9	D9	--- -DACK0
-MEMW ---	C10	D10	--- DRQ0
-MEMR ---	C11	D11	--- -DACK5
SD8 ---	C12	D12	--- DRQ5
SD9 ---	C13	D13	--- -DACK6
SD10 ---	C14	D14	--- DRQ6
SD11 ---	C15	D15	--- -DACK7
SD12 ---	C16	D16	--- DRQ7
SD13 ---	C17	D17	--- +5 VDC
SD14 ---	C18	D18	--- -MASTER
SD15 ---	C19	D19	--- GND
Not Used ---	C20	D20	--- GND

Figure 3-8 CN3: 40-Pin PC/104 Connector Bus C & D Signal

(3) PC/104 Channel Signal Description

Name	Description
AEN [output]	The DMA Address Enable is high when the DMA controller is driving the address bus. It is low when the CPU is driving the address bus
BALE [Output]	The Buffered Address Latch Enable is used to latch SA0 - SA19 onto the falling edge. This signal is forced high during DMA cycles
BUSCLK [Output]	The BUSCLK signal of the I/O channel is asynchronous to the CPU clock.
-DACK 0-3, 5-7 [Output]	The DMA Acknowledges 0 to 3, 5 to 7 are the corresponding acknowledge signals for DRQ 0 to 3 and 5 to 7
DRQ 0-3, 5-7 [Input]	DMA Request channels 0 to 3 are for 8-bit data transfers. DMA Request channels 5 to 7 are for 16-bit data transfers. DMA request should be held high until the corresponding DMA has been completed. DMA request priority is in the following sequence:(Highest) DRQ 0, 1, 2, 3, 5, 6, 7 (Lowest)
-IOCHCK [Input]	The I/O Channel Check is an active low signal which indicates that a parity error exist on the I/O board
IOCHRDY [Input, Open collector]	This signal lengthens the I/O, or memory read/write cycle, and should be held low with a valid address
-IOCS16 [Input, Open collector]	The I/O Chip Select 16 indicates that the present data transfer is a 1-wait state, 16-bit data I/O operation
-IOR [Input/Output]	The I/O Read signal is an active low signal which instructs the I/O device to drive its data onto the data bus
-IOW [Input/Output]	The I/O write signal is an active low signal which instructs the I/O device to read data from the data bus
IRQ 3-7, 9-12, 14, 15 [Input]	The Interrupt Request signal indicates I/O service request attention. They are prioritized in the following sequence : (Highest) IRQ 9, 10, 11, 12, 13, 15, 3, 4, 5, 6, 7 (Lowest)
LA17 - LA23 [Input/Output]	The Unlatched Address line run from bit 17 to 23
-MASTER [Input]	The MASTER is the signal from the I/O processor which gains control as the master and should be held low for a maximum of 15 microseconds or system memory may be lost due to the lack of refresh
-MEMCS16 [Input, Open collector]	The Memory Chip Select 16 indicates that the present data transfer is a 1-wait state, 16-bit data memory operation
-MEMR [Input/Output]	The Memory Read signal is low while any memory location is being read
-MEMW [Input/Output]	The Memory Write signal is low while any memory location is being written
OSC [Output]	The Oscillator is a 14.31818 MHz signal used for the color graphic card
-REFRESH [Input/Output]	This signal is used to indicate a memory refresh cycle and can be driven by the microprocessor on the I/O channel
RSTDRV [Output]	This signal goes high during power-up, low line-voltage or hardware reset
SA0 - SA19 [Input / Output]	The System Address lines run from bit 0 to 19. They are latched onto the falling edge of "BALE"
SBHE [Input/Output]	The System Bus High Enable indicates the high byte SD8 - SD15 on the data bus

Name	Description
SD0 - SD15 [Input/Output]	System Data bit 0 to 15
-SMEMR [Output]	The System Memory Read is low while any of the low 1 mega bytes of memory are being used
-SMEMW [Output]	The System Memory Write is low while any of the low 1 mega bytes of memory is being written
TC [Output]	Terminal Count provides a pulse when the terminal count for any DMA channel is reached
-ZWS [Input, Open collector]	The Zero Wait State indicates to the microprocessor that the present bus cycle can be completed without inserting an additional wait cycle

Table 3-1 I/O Channel Signal's Description

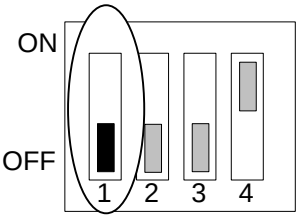
3.2.5 Power / Watch Dog LED (LED1)

The AR-B1420 provides a rectangular LED indicator to indicate the status of the Power/ Watch Dog. LED1 is located at the upper right corner of the board above the 50-pin multi-function port connector.

3.2.6 Serial Port

The RS-232 connectors are integrated into the 50-pin multi-function port connector (CN5).

(1) COM1: RS-232/RS-485 Select (SW1-Switch1)

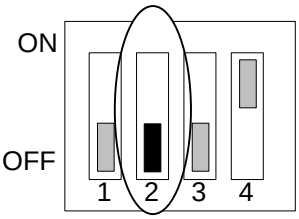


SW1- Switch 1
On: RS-485
Off: RS-232 (Factory Default Setting)

Figure 3-9 COM1: RS-485/RS-422 Connector

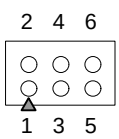
NOTE: 1. The recommended configuration for the RS-485 interface is to set the transmitter to be controlled by DTR to set the transmitter. The receiver is then disabled.

(2) COM2: RS-232/RS-485 Select (SW1-Switch2)



SW1- Switch 2
On: RS-485
Off: RS-232 (Factory Default Setting)

Figure 3-10 COM2: RS-485/RS-422 Connector



1 ANET+
2 BNET+
3 ANET-
4 BNET-
5 GND
6 GND

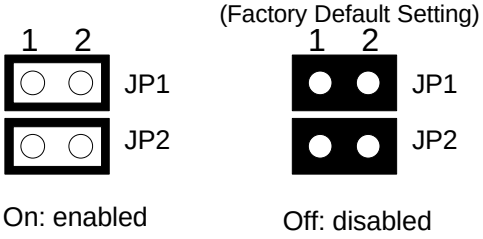
Figure 3-11 J3: RS-485 Pin Jack Assignment

J3	Signal	J3	Signal
1	ANET+	2	BNET+
3	ANET-	4	BNET-
5	GND	6	GND

Table 3-2 RS-485 Pin Assignments

(3) RS-485 Terminator Select (JP1/JP2)

RS-485 may need to be terminated when there are multiple blocks on one line.



On: enabled

Off: disabled

Figure 3-12 J4: RS-485 Terminator Select

3.2.7 TTL Connector (J4)

The TTL I/O port address is at 216H at the I/O port address map.

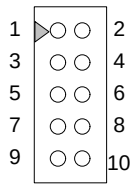


Figure 3-13 J4: TTL Connector

J4	Signal	J4	Signal
1	TTL/OP0	2	TTL/IP0
3	TTL/OP1	4	TTL/IP1
5	TTL/OP2	6	TTL/IP2
7	TTL/OP3	8	TTL/IP3
9	GROUND	10	VCC

Table 3-3 TTL Pin Assignments

3.2.8 Keyboard and PS/2 Mouse Connector (J1)

J1 is used to interface with PS/2 type keyboard /mouse connectors with a 6-pin adapter cable included in the package.

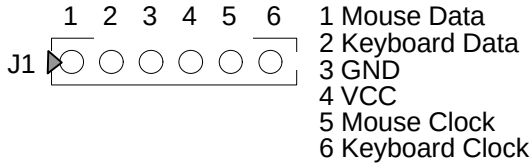


Figure 3-14 J1: Keyboard and PS/2 MouseConnector

3.2.9 External Speaker Header (J2)

The AR-B1420 provides an external speaker header.

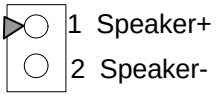


Figure 3-15 J2: Speaker Header

3.2.10 Power Connector (J7)

J7 is a 4-pin power connector. You can directly connect the power supply to the onboard power connector for stand-alone applications.

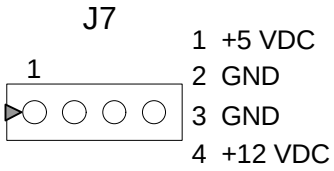


Figure 3-16 J7: 4-Pin Power Connector

3.2.11 Reset Header (J6)

The J6 is used to connect to an external reset switch. Shorting these two pins will reset the system.

Figure 3-17 J6: Reset Header

3.2.12 Battery Setting

(1) Battery Select (JP3)

There is a non-rechargeable battery already on-board. It is not recommended to change this setting. When the computer does not use the SRAM, it does not use the battery, which should last about two to three years without changing.

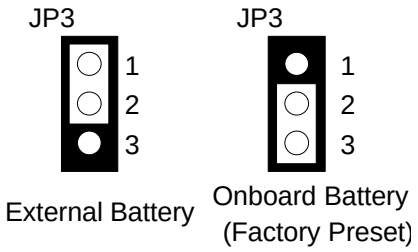


Figure 3-18 JP3: Battery Charger Select

(2) External Battery Connector (J5)

The J5 allows users to connect an external 4.5 to 6-VDC battery to the AR-B1420. The on-board battery must be fully discharged. Only the SRAM disk will draw the battery current. If no SRAM chips are being used, no battery is needed. The battery charger on AR-B1420 does not source charge current to the external battery, which is connected to J5.

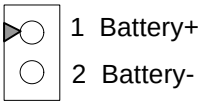


Figure 3-19 J5: External Battery Connector

3.2.13 CPU

The AR-B1420 accepts 486DX series microprocessors such as 66MHz /75MHZ/ 120 MHz. The standard model is built in 66 MHz micro-processor. All of these CPUs include an integer processing unit, a floating-point processing unit, a memory-management unit, and 8 KB cache. They can give a two to ten-fold performance improvement in speed over the 386 processor, depending on the clock speeds used and specific application. Like the 386 processor, the 486 processor includes both segment-based and page-based memory protection schemes. The instruction of processing time is reduced by on-chip instruction pipelining. By performing fast, on-chip memory management and caching, the 486 processor relaxes requirements for memory response for a given level of system performance.

The standard AR-B1420 is embedded with a 66 MHz CPU. No jumper setting or BIOS setup is required for CPU setup.

4. SYSTEM INSTALLATION

This chapter describes the procedure for VGA utility diskette installation. The following topics are covered:

- Overview
- Utility Diskette
- Watch Dog Timer Setup

4.1 OVERVIEW

This chapter provides information for you to set up a working system based on the AR-B1420 CPU board. Please carefully read the details of the CPU board's hardware descriptions before installation, especially the jumper settings, switch settings and cable connections.

Follow the steps listed below for proper installation:

Step 1 : Read the CPU card's hardware description in this manual.

Step 2 : Install SoDIMM onto the CPU card at the rear side of the board.

Step 3 : Set jumpers.

Step 4 : Make sure that the power supply connected to your passive CPU board is turned off.

Step 5 : Plug the CPU card into a free PC/104 slot on the backplane and secure it in place with a screw to the system chassis.

Step 6 : Connect all necessary cables. Make sure that the FDC, HDC, serial and parallel cables are connected to "pin 1" of the related connector.

Step 7 : Connect the hard disk/floppy disk flat cables from the CPU card to the drives. Connect a power source to each drive.

Step 8 : Plug the keyboard into the keyboard connector.

Step 9 : Turn on the power.

Step 10: Configure your system with the BIOS Setup program then re-boot your system.

Step 11: If the CPU card does not work, turn off the power and read the hardware description carefully again.

Step 12: If the CPU card still does not perform properly, return the card to your dealer for immediate service.

4.2 UTILITY DISKETTES

AR-B1420 provides two VGA driver diskettes, supporting WIN31(English version only) and WIN95 as well as the Watchdog Timer program. If your operating system is neither WIN31 nor WIN95 or above, please contact Acrosser so that we can provide proper technical support.

There is one diskette including both drivers for WIN31 and WIN95 VGA resolution. When you extract the compressed files, there is a README file in each sub-directory. Please refer to the README file for any troubleshooting before installing the driver.

4.2.1 VGA Driver

(1) WIN 31 Driver

For the WIN31 operating system, the user must decompress the compressed files in DOS mode. And then follow these steps:

Step 1: Create a new directory for the VGA drivers.
```
C:\>MD VGAWIN31
```

Step 2: Insert the Utility Disk in the floppy disk drive, and then copy the compressed file –Uma31.exe in the newly created directory.
```
C:\>COPY A:\VGAWIN31.EXE C:\VGAWIN31
```

Step 3: Change the working directory to the newly created directory, and extract the compressed file.
```
C:\>CD VGAWIN31
C:\VGAWIN31>VGAWIN31
```
Then, the system will auto-execute the VGAWIN31.exe.

Step 4: Enter WIN31 operation system. Select <Windows Setup> icon from <Main> in the main menu. A sub-menu pops up and you can select the item <Options> and choose <Change System Settings ...> Another popup menu is shown.

Step 5: In the popup menu, choose <Display>. Select <Other Display {required disk from OEM} ..>. A dialog box appears and requests the driver path. Insert the below driver path.
```
C:\VGAWIN31
```
Now, the system will proceed to execute the driver.

Step 6: After the VGA driver finishes executing the driver, it adds all the selectable resolutions. You can choose a proper display resolution according to your own demands.

Step 7: After the system auto-enters DOS mode. Go to the WIN31 sub-directory. Use the editing program to edit the <Display> item in the "System.INI" file. Add the line <Redundancy=OFF> and finally save the change.

Step 8: Re-enter the WIN31 operation system. You now have successfully installed the VGA driver!

Note: Chipset of AR-B1420 is only compatible with the WIN31English version, and the Chinese version is not acceptable.

(2) WIN 95 Driver

For the WIN95 operating system, the user must decompress the compressed files in DOS mode. And then follow these steps:

Step 1: Create a new directory for the VGA drivers.
```
C:\>MD VGAWIN95
```

Step 2: Insert the Utility Disk in the floppy disk drive, and then copy the compressed file –VGAWIN95.exe in the newly created directory.
```
C:\>COPY A:\VGAWIN95.EXE C:\VGAWIN95
```

Step 3: Change the working directory to the newly created directory, and extract the compressed file.
```
C:\>CD VGAWIN95
C:\VGAWIN95>VGAWIN95
```
Then, the system will auto-execute the VGAWIN95.exe.

Step 4: Enter the WIN95 operation system. Please choose the <SETTING> item of the <DISPLAY> icon in the {CONTROL PANEL}. Please select the <From Disk Install> item, and type the factory source files' path.
```
C:\VGAWIN95
```

Step 5: And then you can find the <SGS-THOMSON SPTC> item, select it and click the <OK> button.

Step 6: Finally, you can find the <DISPLAY> icon and then the <Chips> item. You can select this item, and adjust the <Screen Resolution>, <Refresh Rate>, <Font Size> ..and other functions. Please refer to the messages during installation.

4.3 WATCHDOG TIMER

This section describes how to use the Watchdog Timer, including disabled, enabled, and trigger functions.
The AR-B1420 is equipped with a programmable time-out period watchdog timer. You can use your own program to enable the watchdog timer. Once you have enabled the watchdog timer, the program should trigger the I/O every time before the timer times out. If your program fails to trigger or disable this timer before it times out, e.g. because of a system hang-up, it will generate a reset signal to reset the system. The time-out period can be programmed to be set from 15 to 7635 seconds.

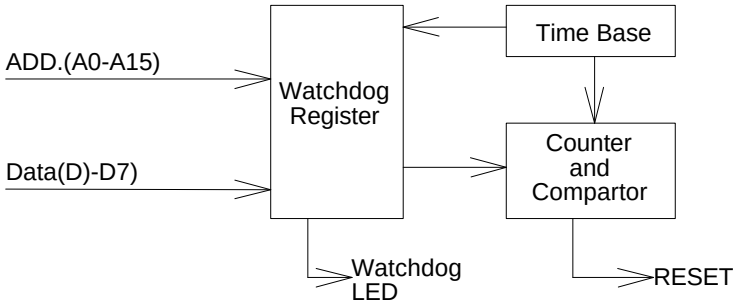


Figure 5-1 Watchdog Block Diagram

The diskette includes a Watch Dog Zip file. In the file, there are 3 execution programs written in different forms. The sub-directories of the file are:
(1) WD-A: Library and Test Program written in Assembly Language
(2) WD-B: Program written in Turbo Basic
(3) WD-C: Library and Test Program written in Turbo C^{++}
The WD-B includes a demonstration program established for users who would like to configure the Watchdog timer by themselves.

4.3.1 Watchdog Timer Setting

The watchdog timer is a circuit that may be used from your program software to detect system crashes or hang-ups. LED1 on this CPU board is the watchdog timer indicator, which is located at the upper-right corner above the 50-pin multi-function connector. Whenever the watchdog timer is enabled, the LED will blink to indicate that the timer is counting. The watchdog timer is automatically disabled after reset.

Once you have enabled the watchdog timer, your program must trigger the watchdog timer every time before it times out. After you trigger the watchdog timer, it will be set to non-zero value to watchdog counter and start to count down again. If your program fails to trigger the watchdog timer before time-out, it will generate a reset pulse to reset the system.

The factor of the watchdog timer time-out constant is approximately 30 seconds. The period for the watchdog timer time-out is between 1 to FF timer factors.

If you want to reset your system when watchdog times out, the following table listed the relation of timer factors between time-out period. The formula of Time-Out Period is 15+30x(Time Factor -1). For example, if the time factor is 10. The Time-out period is calculated as 15+30x(10-1)= 285.

Time Factor	Time-Out Period (Seconds)
1	15
2	30
3	75
4	105
5	135
“	“
“	“
“	“
FF	7635

Table 5-1 Time-out Setting

4.3.2 Watchdog Timer Enabled

To enable the watchdog timer, you have to output a byte of timer factor to the watchdog. The following is a Turbo C^{++} program which demonstrates how to enable the watchdog timer and set the time-out period at 24 seconds.

```
#include “stdio.H”
#include “WATCHDOG.H”

main( )
{
char WD_TIME=ox1;
printf (“Enable watchdog”);
//Set watchdog Timer Output is 15 seconds
_enable_wd (WD_TIME);
}
```

4.3.3 Watchdog Timer Trigger

After you enable the watchdog timer, your program must write the same factor as enabling to the watchdog register at least once every time-out period to its previous setting. You can change the time-out period by writing another timer factor to the watchdog register at any time, and you must trigger the watchdog before the new time-out period in the next trigger. Below is a Turbo C^{++} program which demonstrates how to trigger the watchdog timer:

```
#include “stdio.H”
#include “WATCHDOG.H”

main( )
{
char WD_TIME=ox1;
printf (“Trigger watchdog”);
//Set watchdog Timer Output is 15 seconds
_enable_wd(WD_TIME);
}
```

4.3.4 Watchdog Timer Disabled

To disable the watchdog timer, simply write a 00H to the watchdog register.

```
#include “stadio.H”
#include “WATCHDOG.H”

main ( )
{
printf (“Disable Watch Dog”);
_disable_WD( );
}
```

5.SOLID STATE DISK

The chapter describes SSDs' installation procedures. The following topics are covered:

- Overview
- Switch Settings
- DiskOnChip Installation

5.1 OVERVIEW

The AR-B1420 provides one 32-pin JEDEC DIP socket which may be populated with up to a 1.5 MB flash disk. It is ideal for diskless systems, high reliability and/or high speed access applications, as a controller for industrial or line test instruments, etc.

FLASH function enables you to use 5V FLASH, allowing you to directly program the ROM disk without having to purchase any additional programming equipment to write or erase data. If small page (less or equal 512 bytes per page) 5V FLASHs are used, you can format FLASH disk and copy files onto FLASH disk just like using a floppy disk. If you would like to update 1 or more files to FLASH disk, you just copy these files onto FLASH disk, you don't need to re-program the FLASH disk.

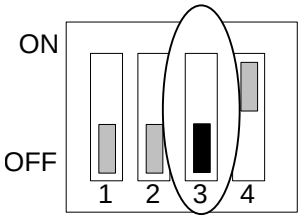
If you are not going to use the solid state disk (SSD), you can use the BIOS setup program to disable the SSD BIOS. The AR-B1420 will not occupy any memory address if the SSD BIOS is disabled.

If you are going to install the EMM386.EXE driver, please use the [X] option to prevent EMM386.EXE from using the particular range of segment address as an EMS page which is used by AR-B9612. For example, write a statement in the CONFIG.SYS file as follows: (If the memory configuration of AR-B9612 is C800:0)

DEVICE=C:\DOS\EMM386.EXE X=C800-CBFF

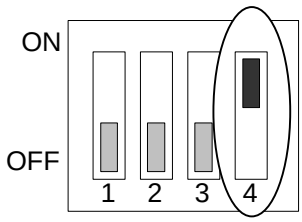
5.2 SWITCH SETTINGS

The AR-B1420 has a built-in 1MB flash disk with 1 socket for DiskOnChip, or an optional 1MB flash memory. The SW1 –Switch 3 –4 is used to configure the S.S.D. settings. Switch 3 is used to select the S.S.D. data bank, and Switch 4 is used to select the memory type (either flash or D.O.C) used in the system.



SW1- Switch 3
On: D000
Off: C800 (Default Setting)

Figure 5-1 SSD Data Bank



SW1- Switch 4
On: Socket inserted with DOC (default setting)
Off: Socket inserted with flash Memory

Figure 5-2 S.S.D. and D.O.C. Select

5.3 SOFTWARE PROGRAMMING

You can use the DOS <FORMAT> and <COPY> command to format and copy files. Follow the following steps to format and copy files to the FLASH disk.

Step 1: Turn on your computer, when the screen shows the SSD BIOS menu, please press "[Ctrl] + [_]" keys at the same time during the system boot-up. This enables you to enter the FLASH setup program.

Step 2: Use <Page-Up>, <Page-Down>, <Right>, and <Left> arrow keys to select the correct FLASH memory type and how many memory chips are going to be used.

Step 3: Press the [F4] key to save the current settings.

Step 4: After the DOS is loaded, use the DOS [FORMAT] command to format the FLASH disk

To format the disk and copy DOS system files to the disk.
C:\>FORMAT [ROM disk letter] /S /U

To format the disk without copying DOS system files.
C:\>FORMAT [ROM disk letter] /U

Step 5: Copy your program or files to the FLASH disk by using the DOS [COPY] command.

CAUTION: It is not recommended that the user format the disk and copy files to the FLASH disk very often. Since the FLASH EPROM's write cycle life time is from 10,000 to 100,000 times, writing data to the FLASH EPROM chips will reduce the life time of the FLASH EPROM chips.

5.4 DISKONCHIP INSTALLATION

The DiskOnChip is a new generation of high performance single-chip Flash Disk. It provides a Flash Disk in a standard 32-pin DIP package.
This unique data storage solution offers a better, faster, and more cost-effective Flash Disk for Single Board embedded systems. The DiskOnChip provides a Flash Disk that does not require any bus, slot or connector. Simply insert the DiskOnChip into the 32-pin socket on the CPU board. It is the optimal solution for single board computers, it is a small, fully functional, easy to integrate, plug-and-play Flash Disk with a very low power consumption.

(1) DiskOnChip Hardware Installation

Step 1: Make sure the target platform's power is OFF

Step 2: Select the SW1 Switch 4 to <ON> to enable the D.O.C.

Step 3: Plug the DiskOnChip device into the socket. Verify that the direction is correct and that Pin1 is lined up with Hole1 on the socket.

Step 4: Line up and insert the AR-B1420 card into any free slot on your computer.

Step 5: Power up the system.

Step 6: During power up you may observe the messages displayed by the DiskOnChip when its drivers are automatically loaded into the system's memory.

Step 7: At this stage the DiskOnChip can be accessed like any disk in the system

Step 8: If the DiskOnChip is the only disk in the system, it will appear as the first disk (drive C: in DOS)

Step 9: If there are more disks besides the DiskOnChip, it will appear by default as the last drive, unless it was programmed as the first drive.

Step 10: If you want the DiskOnChip to be bootable, copy the operating system files into the DiskOnChip by using the standard DOS commands.

(2) Configuring the DiskOnChip as a Bootable Disk

The DiskOnChip fully supports BOOT capabilities. In order for the DiskOnChip to be bootable, it should be DOS formatted as bootable, like any floppy or hard disk that is required to be booted.

SYS D: This command changes the disk into a bootable disk (assuming the DiskOnChip is disk D for this eample)

6. BIOS CONSOLE

This chapter describes the AR-B1420 BIOS menu displays and explains how to perform common tasks needed to get up and running, and presents detailed explanations of the elements found in each of the BIOS menus. The following topics are covered:

- BIOS Setup Overview
- Standard CMOS Setup
- Advanced CMOS Setup
- Advanced Chipset Setup
- Power Management
- PCI/Plug and Play
- Peripheral Setup
- Auto-Detect Hard Disks
- Password Setting
- Load Default Setting
- BIOS Exit
- BIOS Update

6.1 BIOS SETUP OVERVIEW

BIOS is a program used to initialize and set up the I/O system of the computer, which includes the ISA bus and connected devices such as the video display, diskette drives, and the keyboard.

The BIOS provides a menu-based interface to the console subsystem. The console subsystem contains special software, called firmware that interacts directly with the hardware components and facilitates interaction between the system hardware and the operating system.

The BIOS Default Values ensure that the system will function at its normal capability. In the worst situation the user may have corrupted the original settings set by the manufacturer.

After the computer is turned on, the BIOS will perform a diagnostics of the system and display the size of the memory that is being tested. Press the [Del] key to enter the BIOS Setup program, and then the main menu will show on the screen.

The BIOS Setup main menu includes some options. Use the [Up/Down] arrow key to highlight the option that you wish to modify, and then press the [Enter] key to assure(choose) the option and configure the functions.

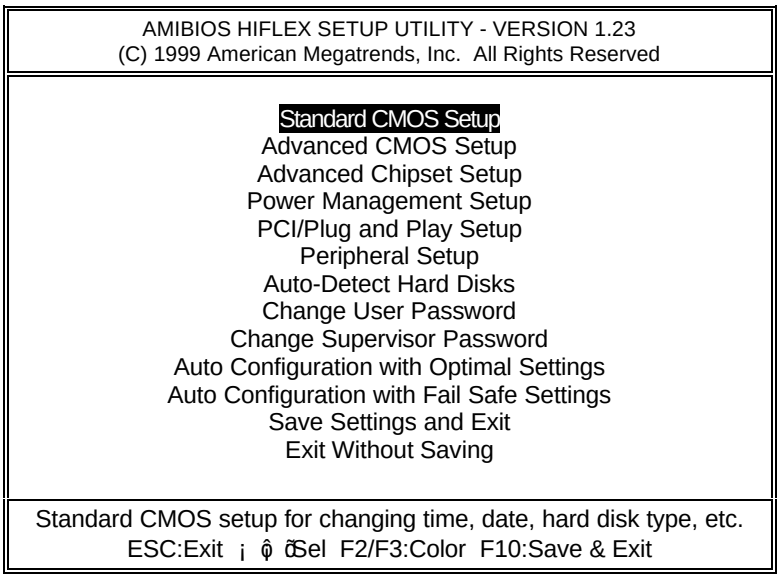


Figure 6-1 BIOS: Setup Main Menu

CAUTION: 1. The AR-B1420 BIOS factory-default setting is set to the <Auto Configuration with Optimal Settings> Acrosser recommends using the BIOS default setting, unless you are very familiar with the settings' functions, or you can contact the technical support engineer at Acrosser.
2. If the BIOS losses the setting, the CMOS will detect the <Auto Configuration with Fail Safe Settings> to boot the operation system, this option will reduce the performance of the system. Acrosser recommends choosing the <Auto Configuration with Optimal Setting> in the main menu. The option has best-case values that should optimize system performance.
3. The BIOS settings are described in detail in this section.

6.2 STANDARD CMOS SETUP

The <Standard CMOS Setup> option allows you to record some basic system hardware configuration and set the system clock and error handling. If the CPU board is already installed in a working system, you will not need to select this option anymore.

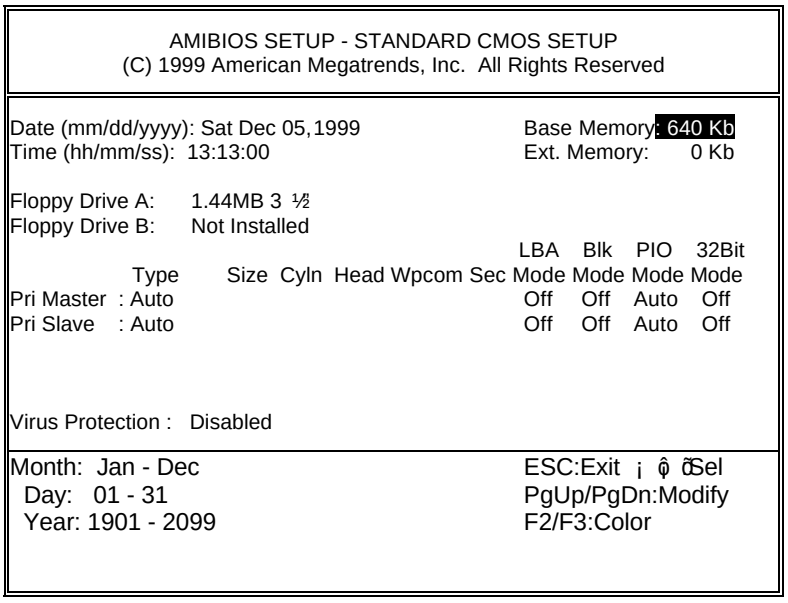


Figure 6-2 BIOS: Standard CMOS Setup

Date & Time Setup

Highlight the <Date> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the same process for the month, day and year format.
Highlight the <Time> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the hour, minute and second format.
The user can bypass the date and time prompts by creating an AUTOEXEC.BAT file. For information on how to create this file, please refer to the MS-DOS manual.

Floppy Setup

The <Standard CMOS Setup> option records the types of floppy disk drives installed in the system.
To enter the configuration value for a particular drive, highlight its corresponding field and then select the drive type using the left-or right-arrow key.

Hard Disk Setup

The BIOS supports various types of USER settings, The BIOS supports <Pri Master> and <Pri Slave> so the user can install up to two hard disks. For the master and slave jumpers, please refer to the hard disk's installation descriptions and the hard disk's jumper settings.
You can select <AUTO> under the <TYPE> and <MODE> fields. This will enable auto detection of your IDE drives during bootup. This will allow you to change your hard drives (with the power off) and then power on without having to reconfigure your hard drive type. If you use older hard disk drives which do not support this feature, then you must configure the hard disk drive in the standard method as described above by the <USER> option.

Boot Sector Virus Protection

This option protects the boot sector and partition table of your hard disk against accidental modifications. Any attempt to write to them will cause the system to halt and display a warning message. If this occurs, you can either allow the operation to continue or use a bootable virus-free floppy disk to reboot and investigate your system. The default setting is <***Disabled***>. This setting is recommended because it can conflict with new operating systems. Installation of new operating system requires that you disable this to prevent write errors.

6.3 ADVANCED CMOS SETUP

The <Advanced CMOS SETUP> option consists of configuration entries that allow you to improve your system performance, or let you set up some system features according to your preference. Some entries here are required by the CPU board's design to remain in their default settings. It is suggested that you leave the settings on their factory defaults unless you are well versed in BIOS features.

AMIBIOS SETUP - ADVANCED CMOS SETUP
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Quick Boot	Disabled	Available Options :
1st Boot Device	IDE-0	Disabled
2nd Boot Device	Floppy	Enabled
3rd Boot Device	CDROM	
4th Boot Device	Disabled	
Try Other Boot Devices	Yes	
Floppy Access Control	Normal	
Hard Disk Access Control	Normal	
S.M.A.R.T. for Hard Disks	Disabled	
BootUp Num-Lock	On	
Floppy Drive Swap	Disabled	
Floppy Drive Seek	Disabled	
PS/2 Mouse Support	Enabled	
Typematic Rate	Fast	
System Keyboard	Absent	
Primary Display	Absent	
Password Check	Setup	
Boot to OS/2	No	
Wait For 'F1' If Error	Enabled	
Hit 'DEL' Message Display	Enabled	
Internal Cache	WriteBack	
System BIOS Cacheable	Enabled	
C000, 16k Shadow	Enabled	
C400, 16k Shadow	Enabled	
C800, 16k Shadow	Disabled	
CC00, 16k Shadow	Disabled	
D000, 16k Shadow	Disabled	
D400, 16k Shadow	Disabled	
D800, 16k Shadow	Disabled	ESC:Exit Sel
DC00, 16k Shadow	Disabled	PgUp/PgDn:Modify
INTERNAL_FLASH_DISK	CC000H	F2/F3:Color

Figure 6-3 BIOS: Advanced CMOS Setup

Quick Boot

This category speeds up Power On Self Test (POST) after you power on the computer. If it is set to ***Enabled***, BIOS will shorten or skip some check items during POST.

1st Boot Device
2nd Boot Device
3rd Boot Device
4th Boot Device
Try Other Boot Devices

These options determine which device the system searches first for an operating system during boot-up. When "Try Other Boot Devices" is set to "Yes," the system will search this device first than the above other devices.

Floppy Access Control

This option specifies the floppy access to be "read/write" (normal) or "read only."

Hard Disk Access Control

This option specifies the hard disk access to be "read/write" (normal) or "read only."

BootUp Num-Lock

This item is used to activate the Num-Lock function upon system bootup. If the setting is on, after a boot, the Num-Lock light is lit, and user can use the number key.

Floppy Drive Swap

The option reverses the drive letter assignments of your floppy disk drives in the Swap A, B setting, otherwise leave on the setting of ***Disabled*** (No Swap). This works separately from the BIOS Features floppy disk swap feature. It is functionally the same as physically interchanging the connectors of the floppy disk drives. When <***Enabled***>, the BIOS swapped floppy drive assignments so that Drive A becomes Drive B, and Drive B becomes Drive A under DOS.

Floppy Drive Seek

If the <Floppy Drive Seek> item is setting ***Enabled***, the BIOS will seek the floppy <A> drive one time upon bootup.

PS/2 Mouse Support

The setting of ***Enabled*** allows the system to detect a PS/2 mouse on bootup. If detected, IRQ12 will be used for the PS/2 mouse. IRQ 12 will be reserved for expansion cards if a PS/2 mouse is not detected. ***Disabled*** will reserve IRQ12 for expansion cards and therefore the PS/2 mouse will not function.

Typematic Rate

This item specifies the speed at which a keyboard keystroke is repeated.

System Keyboard

This function specifies that a keyboard is attached to the computer.

Primary Display

The option is used to set the type of video display card installed in the system.

Password Check

This option enables password checking every time the computer is powered on or every time the BIOS Setup is executed. If ***Always*** is chosen, a user password prompt appears every time the computer is turned on. If ***Setup*** is chosen, the password prompt appears if the BIOS executed.

Boot to OS/2

When using the OS/2 operating system with installed DRAM of greater than 64MB, you need to ***Enabled*** this option otherwise leave this on the setup default of ***Disabled***.

Wait for 'F1' If Error

AMIBIOS POST error messages are followed by:

```
Press <F1> to continue
```

If this option is set to ***Disabled***, the AMIBIOS does not wait for you to press the <F1> key after an error message.

Hit 'DEL' Message Display

Set this option to ***Disabled*** to prevent the message as follows:

```
Hit 'DEL' if you want to run setup
```

It will prevent the message from appearing on the first BIOS screen when the computer boots.

Internal Cache

This option specifies the caching algorithm used for L1 internal cache memory. The settings are:

Setting	Description
Disabled	Neither L1 internal cache memory on the CPU or L2 secondary cache memory is enabled.
WriteBack	Use the write-back caching algorithm.
WriteThru	Use the write-through caching algorithm.

Table 6-1 Internal Cache Setting

System BIOS Cacheable

When this option is set to ***Enabled***, the contents of the F0000h system memory segment can be read from or written to L2 secondary cache memory. The contents of the F0000h memory segment are always copied from the BIOS ROM to system RAM for faster execution.

The settings are ***Enabled*** or ***Disabled***. The Optimal default setting is ***Enabled***. The Fail-Safe default setting is ***Disabled***.

C000, 16k Shadow
C400, 16k Shadow
C800, 16k Shadow
CC00, 16k Shadow
D000, 16k Shadow
D400, 16k Shadow
D800, 16k Shadow
DC00, 16k Shadow

These options control the location of the contents of the 16KB of ROM beginning at the specified memory location. If no adapter ROM is using the named ROM area, this area is made available to the local bus. The settings are:

SETTING	DESCRIPTION
Disabled	The video ROM is not copied to RAM. The contents of the video ROM cannot be read from or written to cache memory.
Enabled	The contents of C000h - C7FFFh are written to the same address in system memory (RAM) for faster execution.
Cached	The contents of the named ROM area are written to the same address in system memory (RAM) for faster execution, if an adapter ROM will be using the named ROM area. Also, the contents of the RAM area can be read from and written to cache memory.

Table 6-2 Shadow Setting

INTERNAL_FLASH_DISK

This option selects the SSD BIOS memory address.

6.4 ADVANCED CHIPSET SETUP

This option controls the configuration of the board's chipset. Control keys for this screen are the same as for the previous screen.

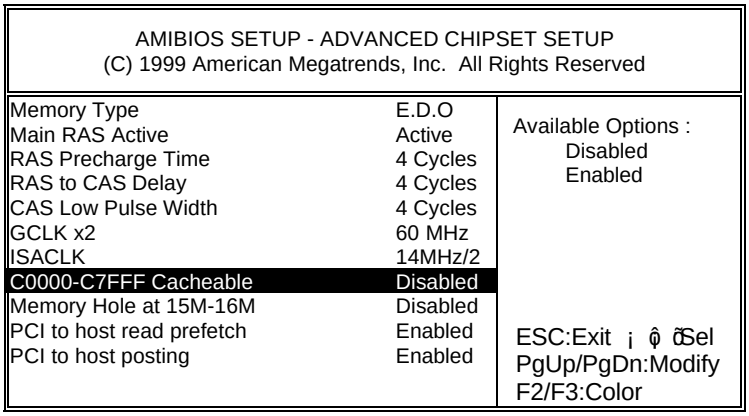

Figure 6-4 BIOS: Advanced Chipset Setup

Memory Type

There are 2 memory types: E.D.O. and Fast page. Specify the type used in the system.

Main RAS Active

The option controls if RAS is kept active after the current DRAM access.

RAS Precharge Time

This controls the idle clocks after issuing a precharge command to DRAM.

RAS to CAS Delay

This controls the latency between DRAM active command and the read/write command.

CAS Low Pulse Width

The 4 items are related to system memory internal operation. It is recommended to use the default settings.).

GCLKx2

This option is used to select the VGA bus clock rate.

ISACLK

This option is used to select the system ISA clock rate

Memory Hole at 15-16M

This option specifies the range 15MB to 16MB in memory that cannot be addressed on the ISA bus.

PCI to host read precharge

This option controls if all burst reads from a PCI master addressed to the East Bridge system memory will use the prefetch function.

PCI to host posting

This option controls if the memory writes from a PCI master addressed to the East Bridge system memory can be posted.

6.5 POWER MANAGEMENT

This section is used to configure power management features. This <Power management Setup> option allows you to reduce power consumption. This feature turns off the video display and shuts down the hard disk after a period of inactivity.

AMIBIOS SETUP - Power Management Setup
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Power Management /APM	Disabled
Video Power Down Mode	Disabled
Hard Disk Power Down Mode	Disabled
Hard Disk Time Out (Minute)	Disabled
Doze Time Out (Second)	Disabled
Standby Time Out (Minute)	Disabled
Suspend Time Out (Minute)	Disabled
Full-On Clock Throttle Ratio	Normal Clock
Power –Down Clock Throttle Ratio	Normal Clock
STPCLK# Modulation Period	64 us
Display Activity	Ignore
DMA Activity	Ignore
PCI Master Activity	Ignore
Parallel IO Activity	Monitor
Serial IO Activity	Monitor
Keyboard Activity	Monitor
Floppy Disk Activity	Ignore
Hard Disk Activity	Ignore
IRQ1 – 15 Interrupt	Monitor
System Timer Interrupt	Ignore
NMI Interrupt	Ignore

Available Options :
Disabled
Enabled

ESC:Exit Sel
PgUp/PgDn:Modify
F2/F3:Color

Figure 6-5 BIOS: Power Management Setup

Power Management /APM

This option is to enable the power management and APM (Advanced Power Management) features.

Video Power Down Mode

This option specifies the power management states that the hard disk drive enters after the specified period of display inactivity has expired.

Hard Disk Power Down Mode

This option specifies the power management states that the hard disk drive enters after the specified period of display inactivity has expired.

Hard Disk Time Out

This option specifies the length of a period of hard disk inactivity. When this period expired, the hard disk drive enters the power-conserving mode specified on the <Hard Disk Power Down Mode> option.

Doze Time Out
Standby Time Out
Suspend Time Out

The 3 options are all related to the system power-saving mode during system inactivity. Normally, if the 3 options are set to "Enabled," the sequence of the power-saving mode is Doze Mode Standby Mode Suspend Mode. In Suspend mode, nearly all power used is curtailed.

BIOS Setup			Power Saving Mode
Doze Time out	**Standby Time out**	**Suspend Time out**	
Enabled	Enabled	Enabled	Doze Standby Suspend
Disabled	Disabled	Disabled	The system will not enter power saving mode.
Any of the options is set to **"Disabled"** with the other 2 **"Enabled."**			The system will sequentially enter the 2 modes set to "Enabled." Remember Doze mode is always the first mode system will enter and Suspend mode is the last.
Any of the options is set to **"Enabled"** with the other 2 **"Disabled."**			The system will only enter the mode that is set to "Enabled."

Table 6-3 Power Saving Mode

Full-On Clock Throttle Ratio

This option increases the system stability when power on. The system clock frequency may be divided when received into the chipset during bootup. .After the system enters the operation system, the frequency division in chipset will not exist and return to normal state.

Power –Down Clock Throttle Ratio

This option is related to the power saving state: Doze/ Standby/ Suspend modes. When the system is in one of these modes, the system clock will reduce the frequency for power saving.

STPCLK# Modulation Period

STPCLK is the system clock. When the option is set to "Enabled," the STPCLK modulation period is 64ms else. If "Disabled," the period is 64us.

Display Activity

This option controls the activity of display device.

DMA Activity

This option controls the activity of DMA device.

PCI Master Activity

This option controls the activity of PCI Master device.

Parallel IO Activity

When the system is in sleep mode, it can be re-started through a printer port device.

Serial IO Activity

When the system is in sleep mode, it is awakened whenever there is an action from COM port-based device.

Keyboard Activity

When the system is in sleep mode, it is awakened whenever there is an action from hard disk through keyboard device.

Floppy Disk Activity

This option controls the activity of floppy disk device.

Hard Disk Activity

This option controls the activity of hard disk device..

IRQ1-15

When the system is in sleep mode, it is awakened whenever there is an action from IRQ1-IRQ15.

System Timer Interrupt

This option controls the activity of system timer interrupt.

NMI Interrupt

This option controls the activity of the signal "NMI" emitted by CPU during power-on

6.6 PCI/PLUG AND PLAY

This section is used to configure PCI / Plug and Play features. The <PCI & PNP Setup> option configures the PCI bus slots. All PCI bus slots on the system use INTA#, thus all installed PCI cards must be set to this value.

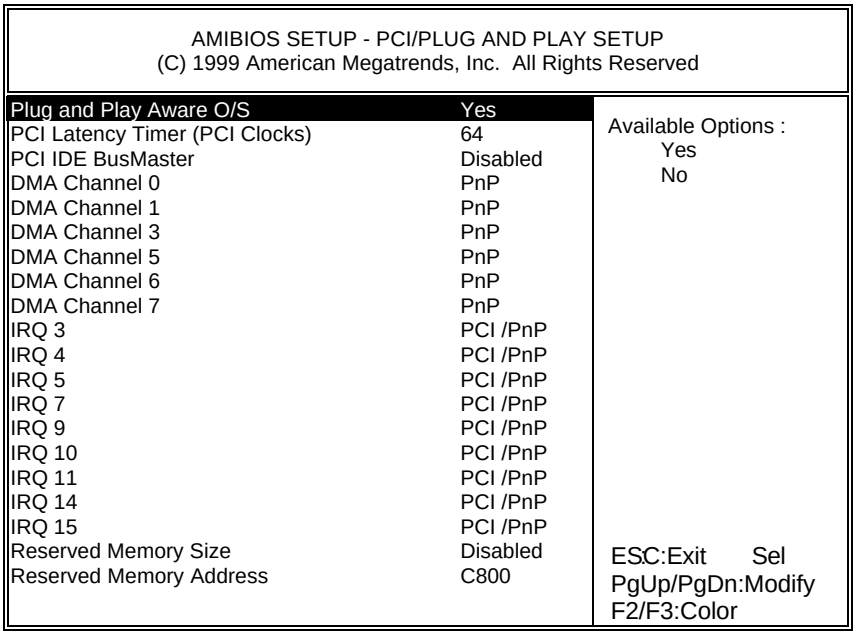


Figure 6-6 BIOS: PCI / Plug and Play Setup

Plug and Play Aware O/S

Set this option to ***Yes*** if the operating system installed in the computer is Plug and Play-aware. The BIOS only detects and enables PnP ISA adapter cards that are required for system boot. The Windows 95 operating system detects and enables all other PnP-aware adapter cards. Windows 95 is PnP-aware. Set this option <***No***> if the operating system (such as DOS, OS/2, Windows 3.x) does not use PnP. You must set this option correctly or PnP-aware adapter cards installed in your computer will not be configured properly.

PCI Latency Timer (PCI Clocks)

This option sets latency of all PCI devices on the PCI bus. The settings are in units equal to PCI clocks.

PCI IDE BusMaster

Enabled this option is to specify that the IDE controller on the PCI local bus has bus mastering capability.

DMA & IRQ

These options specify the bus that the named IRQs/DMAs lines are used on. These options allow you to specify IRQs/DMAs for use by legacy ISA adapter cards. These options determine if the BIOS should remove an IRQ/DMA from the pool of available IRQs/DMAs passed to BIOS configurable devices. If more IRQs/DMAs must be removed from the pool, the end user can use these PCI/PnP Setup options to remove the IRQ/DMA by assigning the option to the ISA/EISA setting. Onboard I/O is configurable by BIOS.

Reserved memory Size

This option specifies the size of the memory area reserved for legacy ISA adapter cards.

Reserved memory Address

This option specifies the beginning address (in hex) of the reserved memory area. The specified ROM memory area is reserved for use by legacy ISA adapter cards.

6.7 PERIPHERAL SETUP

This section is used to configure peripheral features.

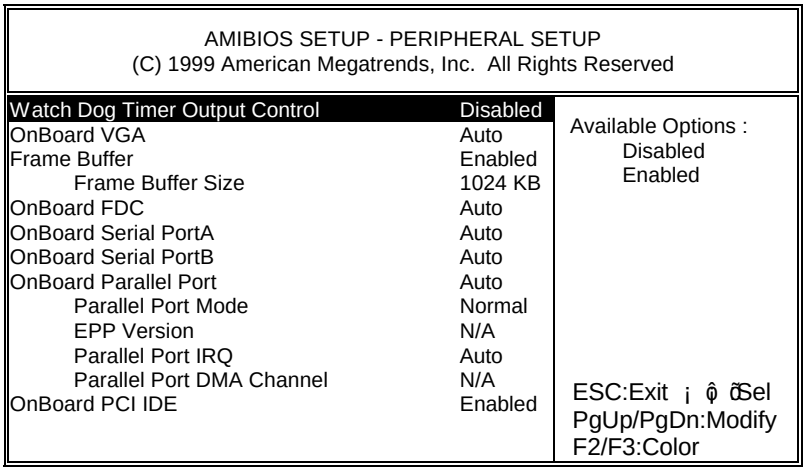


Figure 6-7 BIOS: Peripheral Setup

Watch Dog Timer Output Control

This item controls Watch Dog Timer Output.

OnBoard VGA

This option is to enable the onboard VGA function.

Frame Buffer

This option specifies if the onboard VGA will share the system memory.

Frame Buffer Size

This option is to select the size of VGA memory shared from the system.

Parallel Port Mode

This option specifies the parallel port mode. ECP and EPP are both bidirectional data transfer schemes that adhere to the IEEE1284 specifications.

OnBoard PCI IDE

This option specifies the onboard IDE controller channels that will be used.

6.8 AUTO-DETECT HARD DISKS

This option detects the parameters of an IDE hard disk drive, and automatically enters them into the Standard CMOS Setup screen.

6.9 PASSWORD SETTING

This BIOS Setup has an optional password feature. The system can be configured so that all users must enter a password every time the system boots or when BIOS Setup is executed. The user can set either a Supervisor password or a User password.

6.9.1 Setting Password

Select the appropriate password icon (Supervisor or User) from the Security section of the BIOS Setup main menu. Enter the password and press [Enter]. The screen does not display the characters entered. After the new password is entered, retype the new password as prompted and press [Enter].

If the password confirmation is incorrect, an error message appears. If the new password is entered without error, press [Esc] to return to the BIOS Main Menu. The password is stored in CMOS RAM after the BIOS is completed. The next time the system boots, you are prompted for the password function is present and is enabled.

```
Enter new supervisor password:
```

6.9.2 Password Checking

The password check option is enabled in Advanced Setup by choosing either ***Always*** (the password prompt appears every time the system is powered on) or ***Setup*** (the password prompt appears only when BIOS is run). The password is stored in CMOS RAM. The user can enter a password by typing it on the keyboard. You should select Supervisor or User. The BIOS prompts for a password, the user must set the Supervisor password before the user can set the User password. Enter 1-6 characters as a password. The password does not appear on the screen when typed. Make sure you write it down.

6.10 LOAD DEFAULT SETTINGS

This section permits the user to select a group of settings for all BIOS Setup options. Not only can you use these items to quickly set system configuration parameters, you can choose a group of settings that have a better chance of working when the system is having configuration related problems.

6.10.1 Auto Configuration with Optimal Setting

User can load the optimal default settings for the BIOS. The Optimal default settings are best-case values that should optimize system performance. If CMOS RAM is corrupted, the optimal settings are loaded automatically.

```
Load high performance settings (Y/N) ?
```

6.10.2 Auto Configuration with Fail Safe Setting

User can load the Fail-Safe BIOS Setup option settings by selecting the Fail-Safe item from the Default section of the BIOS Setup main menu.
The Fail-Safe settings provide far from optimal system performance, but are the most stable settings. Use this option as a diagnostic aid if the system is behaving erratically.

```
Load failsafe settings (Y/N) ?
```

6.11 BIOS EXIT

This section is used to exit the BIOS main menu in two types of situation. After making your changes, you can either save them or exit the BIOS menu without saving the new values.

6.11.1 Save Settings and Exit

This item set in the <Standard CMOS Setup>, <Advanced CMOS Setup>, <Advanced Chipset Setup> and the new password (if it has been changed) will be stored in the CMOS. The CMOS checksum is calculated and written into the CMOS.

As you select this function, the following message will appear at the center of the screen to assist you to save data to CMOS and Exit the Setup.

```
Save current settings and exit (Y/N) ?
```

6.11.2 Exit Without Saving

When you select this option, the following message will appear at the center of the screen to help to Abandon all Data and Exit Setup.

```
Quit without saving (Y/N) ?
```

6.12 BIOS UPDATE

The BIOS program instructions are contained within computer chips called FLASH ROMs that are located on your system board. The chips can be electronically reprogrammed, allowing you to upgrade your BIOS firmware without removing and installing chips.

The AR-B1420 BIOS provides a menu-based interface to the console subsystem. The console subsystem contains special software, called firmware that interacts directly with the hardware components and facilitates interaction between the system hardware and the operating system.

The AR-B1420 provides a FLASH BIOS update function for you to easily upgrade to a newer BIOS version. Please follow the operating steps for updating to a new BIOS:

Step 1: Insert the FLASH BIOS diskette into the floppy disk drive.

Step 2: Turn on your system and press [Ctrl]+[Home] (Hit the [Ctrl] key and [Home] key simultaneously just as you power on. Then the onboard BIOS will read new BIOS file name and AMIBOOT.ROM from floppy drive and write to FLASH.

Step 3: If all steps are followed correctly, the system will reboot. But if the system did not boot up, please check everything and try again. If it still does not work, please contact your Acrosser distributor for technology support at once.

NOTE: 1. After turning on the computer and the system has not deteced the boot procedure, please press the [Ctrl]+[Home] key immediately. The system will detect the BIOS file from floppy drive. A quick action is important.

2. The BIOS Flash disk is not a standard accessory. It can be used to add some functions. If it is necessary to use as an update in the future, you can download the suitable BIOS. The address is as follows:

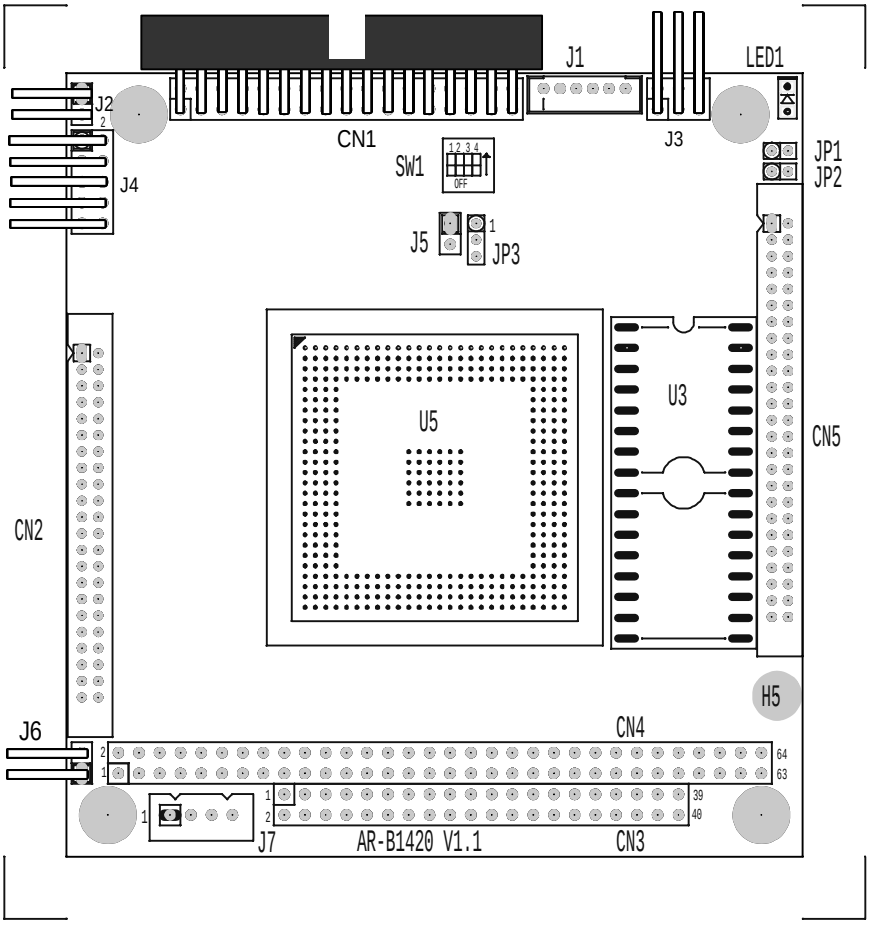
http:\\www.acrosser.com

7. SPECIFICATIONS

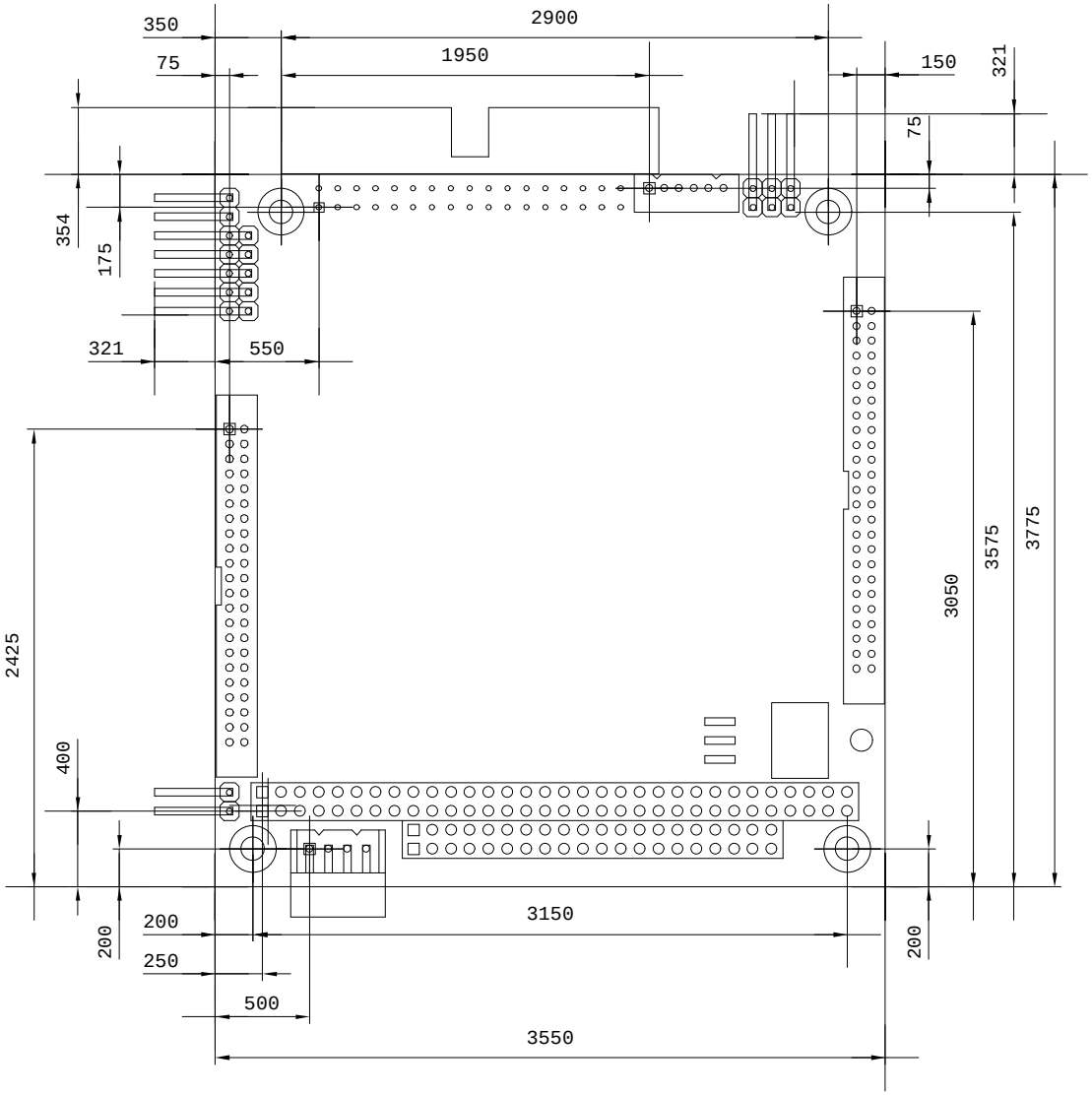
CPU & Chipset	ST STPC Client 66/ 75/120 MHz 486 DX CPU .(Intel 486 DX Grade)
Bus Interface:	Non-stack through PC/104 bus
VGA	Up to 4MB MB VRAM (1280X1024/256 colors)
HDC:	One PCI IDE Supports LBA/Block mode access
FDC:	Supports two 5.25" or 3.5" floppy disk drives
Parallel Port:	1 bi-directional centronics type parallel port Supports SPP/EPP/ECP mode
Serial Port:	2 RS-232C/RS-485
Keyboard:	PC/AT compatible keyboard
Watchdog:	Programmable watchdog timer
Speaker:	External speaker
Real Time Clock:	BQ3287MT or compatible chips with 128 bytes of data RAM
BIOS:	AMI Flash BIOS (128KB, including VGA BIOS)
Flash Disk:	Supports 1 DiskOnChip socket
BUS Drive Cap.:	6 TTL level loads maximum
CE Design-In:	Add EMI components to COM ports, parallel port, CRT, keyboard, and PS/2 mouse
Indicator:	Power/ watchdog LED
Power Req.:	+5V only, 2.0A maximum
PC Board:	8 layers, EMI considered
Dimensions:	90.2 mmX95.9 mm (3.55"X3.775")

8. PLACEMENT & DIMENSIONS

8.1 PLACEMENT



8.2 DIMENSIONS



Unit: mil (1 inch = 25.4 mm = 1000 mil)

9. PROGRAMMING RS-485

The majority of the communicative operations of the RS-485 are the same as the RS-232. When the RS-485 proceeds with the transmission which needs to control the DTR(TXC) signal, the installation steps are as follows:

Step 1: Enable DTR (Data Terminal Relay)

Step 2: Send out data

Step 3: Wait for data to empty

Step 4: Disable DTR

NOTE: Please refer to the section of the "Serial Port" in the chapter "System Control" for the detailed description of the COM port's register.

(1) Initializing the COM port

Step 1: Initialize the COM port in the receiver interrupt mode, and /or transmitter interrupt mode. (All of the communication protocol buses of the RS-485 are the same.)

Step 2: Disable DTR (Data Terminal Relay) the bit 0 of the address of offset+4 just sets to "0".

NOTE: Control the AR-B1420 CPU card's DTR signal to enable/disable the RS-485's TXC communication.

(2) Send out one character (Transmit)

Step 1: Enable the DTR signal, and the bit 0 of the address of offset+4 just sets to "1".

Step 2: Send out the data. (Write this character to the offset+0 of the current COM port address)

Step 3: Wait for the buffer's data to empty. Check the transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) so that all sets are set to "0".

Step 4: Disable the DTR signal, and the bit 0 of the address of offset+4 sets to "0"

(3) Send out one block data (Transmit – the data can be more than two characters long)

Step 1: Enable the DTR signal, and the bit 0 of the address of offset+4 just sets to "1".

Step 2: Send out the data. (Write all data to the offset+0 of the current COM port address)

Step 3: Wait for the buffer's data to empty. Check the transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) so that all sets are set to "0".

Step 4: Disabled DTR signal, and the bit 0 of the address of offset+4 sets to "0"

(4) Receive data

The RS-485's operation of receiving data is the same as RS-232's.

(5) Basic Language Example

a.) Initial 86C450 UART

```
10    OPEN "COM1:9600,m,8,1" AS #1 LEN=1
20    REM Reset DTR
30    OUT &H3FC, (INP(%H3FC) AND &HFA)
40    RETURN
```

b.) Send out one character to COM1

```
10    REM Enable transmitter by setting DTR ON
20    OUT &H3FC, (INP(&H3FC) OR &H01)
30    REM Send out one character
40    PRINT #1, OUTCHR$
50    REM Check transmitter holding register and shift register
60    IF ((INP(&H3FD) AND &H60) >0) THEN 60
70    REM Disable transmitter by resetting DTR
80    OUT &H3FC, (INP(&H3FC) AND &HEF)
90    RETURN
```

c.) Receive one character from COM1

```
10    REM Check COM1: receiver buffer
20    IF LOF(1)<256 THEN 70
30    REM Receiver buffer is empty
40    INPSTR$"
50    RETURN
60    REM Read one character from COM1: buffer
70    INPSTR$=INPUT$(1,#1)
80    RETURN
```

10.INDEX