Aug 16, 2007

FP24-01A-RS-R20

Ordering Information

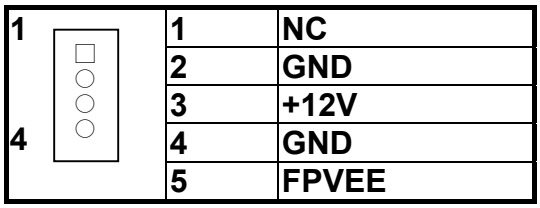
FP24-01A-RS-R20: 50Pin TTL to 44Pin TTL Connector Module

Connectors

J1 : Output Panel interface

PIN NO	FUNCTION	PIN NO	FUNCTION
1	P20	23	LP
2	GND	24	P12
3	P16	25	SHFCLK
4	PLCD	26	P5
5	P21	27	PLCD
6	P0	28	P13
7	P17	29	PLCD
8	P8	30	P6
9	P22	31	ENABLK
10	P1	32	P14
11	P18	33	FPVDD
12	P9	34	P7
13	P23	35	FPVEE
14	P2	36	P15
15	P19	37	GND
16	P10	38	+12V
17	PLCD	39	GND
18	P3	40	+12V
19	FLM	41	NC
20	P11		
21	M		
22	P4		

J2 :Power Connector for backlight inverter

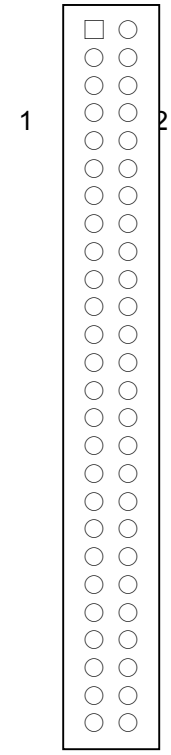


1	NC
2	GND
3	+12V
4	GND
5	FPVEE

J3 : Output Panel interface

PIN NO	FUNCTION	PIN NO	FUNCTION
1	+12V	23	P14
2	+12V	24	P15
3	GND	25	P16
4	GND	26	P17
5	PLCD	27	P18
6	PLCD	28	P19
7	FPVEE	29	P20
8	GND	30	P21
9	P0	31	P22
10	P1	32	P23
11	P2	33	GND
12	P3	34	GND
13	P4	35	SHFCLK
14	P5	36	FLM
15	P6	37	M
16	P7	38	LP
17	P8	39	GND
18	P9	40	ENBKL
19	P10	41	NC
20	P11	42	NC
21	P12	43	FPVDD
22	P13	44	PLCD

J4 : Panel Signal from CPU board (reference)



Signal Name	Pin #	Pin #	Signal Name
NC	1	2	GND
GND	3	4	GND
GND	5	6	GND
GND	7	8	GND
GND	9	10	GND
GND	11	12	GND
GND	13	14	P21
P23	15	16	P22
P16	17	18	P20
P17	19	20	P18
P19	21	22	P14
P13	23	24	P12
P15	25	26	P11
P7	27	28	P10
PLCD	29	30	PLCD
P9	31	32	P8
P4	33	34	P6
P3	35	36	P5
P2	37	38	P1
M	39	40	P0
SHFCLK	41	42	ENABKL
FPVDD	43	44	FLM
FPVEE	45	46	LP
GND	47	48	GND
+12V	49	50	+12V

SHFCLK: Shift Clock. Pixel clock for flat panel data.

FLM: First Line Marker.Flat Panel equivalent of VSYNC.

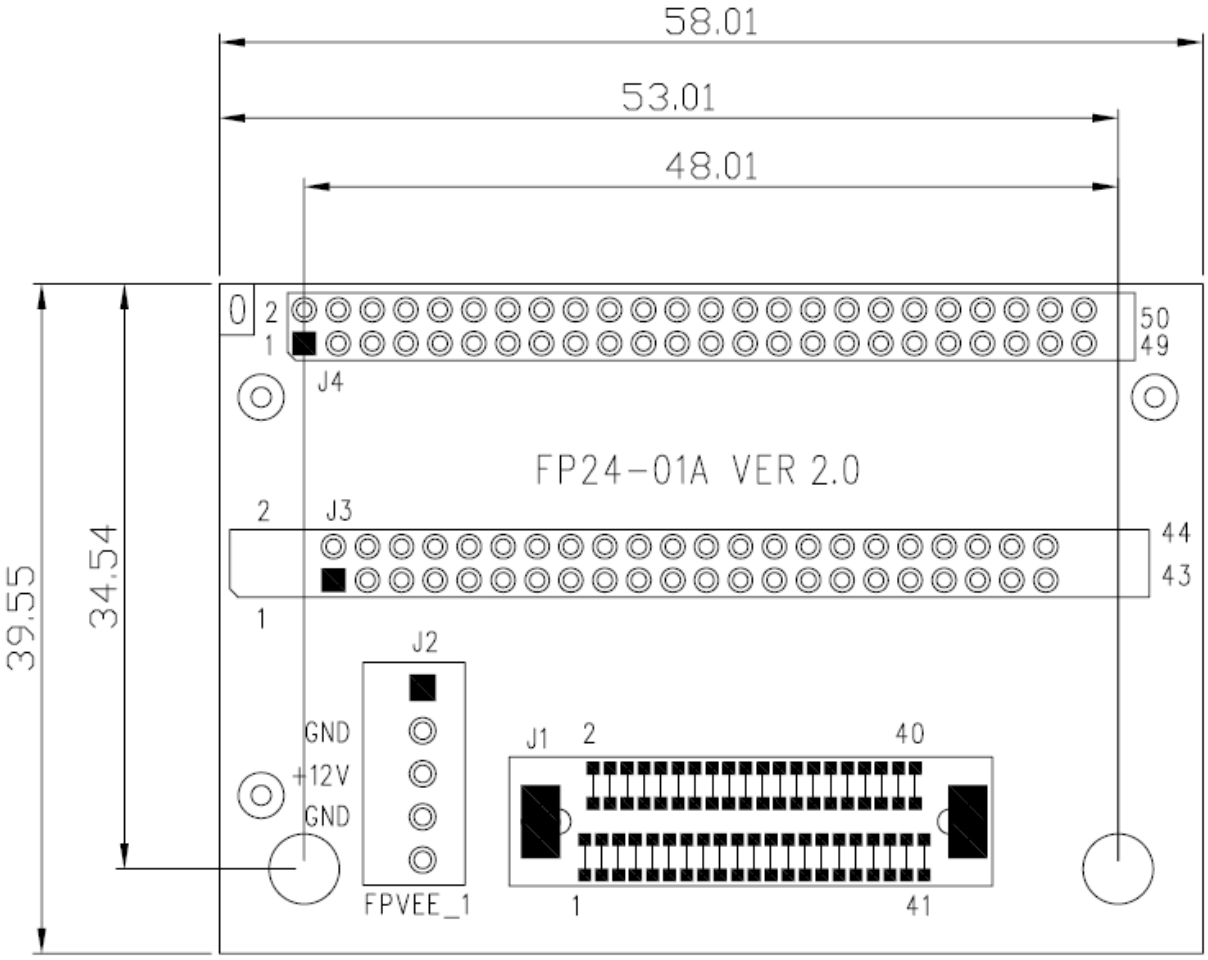
LP: Latch Pulse(may also be called CL1).

M: M signal for panel AC drive control (may also be called ACDCLK).

ENABKL: power sequencing control for enabling the backlight

FPVEE: Power sequencing control for panel bias voltage VEE. May also be configured as ENABKL

Dimension


58.01
53.01
48.01
39.55
34.54
2
1
J4
50
49
FP24-01A VER 2.0
2
J3
44
43
1
J2
GND
+12V
GND
FPVEE_1
J1
2
40
1
41