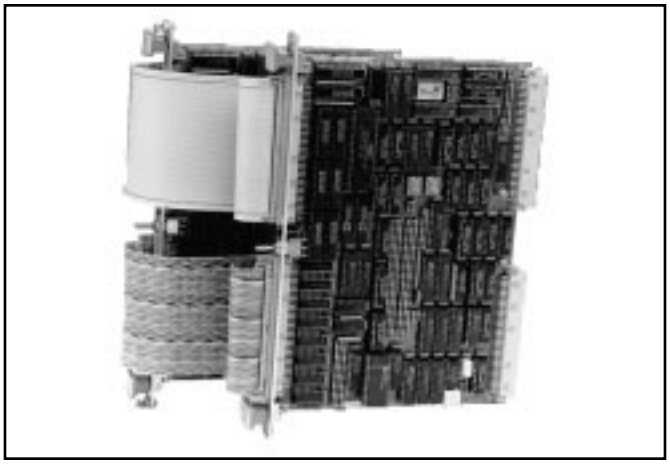
VMIVME-5510L-XX
VMEbus Multimaster Repeater Link

- Multimaster – allows multiple VMEbus masters in all chassis
- Software transparent mode – allows direct communication from primary chassis to secondary chassis with no software overhead (unidirectional link control with bidirectional data transfers)
- In nontransparent mode, link arbiter determines which VMIVME-5510 is master of the link
- In nontransparent mode, single cycle or burst access across the link is selected by software
- Memory protected by user-selectable access window
- Any address window in one chassis can be mapped to any window in the other chassis (for example, extended supervisory to short nonprivileged)
- Window sizes are jumper-selected from 256 bytes to 16 Mbyte (power of two sizes, that is, 256, 512, 1 K, 2 K, etc.)
- Compliant to VMEbus Rev. C.1
- Supports 8-, 16-, and 32-bit addressing (bidirectional)
- Supports 16-, 24-, and 32-bit addressing (bidirectional)
- Program-controlled attention interrupts allow each chassis to interrupt the other chassis
- Supports up to 25-foot cables
- Allows expansion to multiple VMEbus systems in a star configuration
- Switch-controlled isolation for maintenance
- Software-controlled isolation
- Two boards and two cables (in a variety of cable lengths) form a VME-to-VME link
- Automatic detection of remote chassis power up



VMEbus MULTIMASTER REPEATER LINK OVERVIEW — The VMIVME-5510 Link is a high-performance, yet easy-to-use method of linking two or more VMEbus systems together. It is also useful in linking a wide variety of computer systems based on VMEbus or designed with VMEbus front ends.

The link consists of two boards and two cables which enable a VMEbus system to be expanded beyond a single chassis. A functional block diagram is provided in Figure 1. Several options and modes of operation are available to enable the user to optimize a variety of system configurations.

MODES OF OPERATION

Remote Power Up Detection: Each VMIVME-5510 automatically detects the presence/absence of the other VMIVME-5510. If one VMIVME-5510 is not present, transfers across the link initiated by the local chassis are terminated via a software-selectable BERR or DTACK. The default is BERR. In the case of DTACK, an on-board register indicates success or failure of a transfer.

Software Transparent Expansion of VMEbus: The option is jumper-selectable and expands the VMEbus through an address window. A new base address is generated for the secondary chassis. The expanded bus is not accessed by the primary bus unless the address is within the address window. This method allows masters in the primary chassis to operate without the continuous overhead of arbitrating for an expanded bus. This link is software transparent in this mode, that is, it allows for plug-and-play operation with bidirectional data transfers. Note: This mode allows only one repeater board to be Master of the link (see Figure 3).

Multiprocessing Mode: With hardware designed to minimize required control software, this mode provides the flexibility to construct elaborate distributed processor systems and allows the links to be memory mapped in both directions (see Figure 4). On-board jumpers are available to limit map size and/or provide address translation. Thus, accesses from either chassis to the other can be restricted to user-specified areas. Both chassis are automatically interlocked only when the address is within the user-selected window. An arbiter on the primary VMIVME-5510 (primary or secondary is selected by jumpers) determines which

Ordering Options	
June 7, 1999 800-005510-000 E	
VMIVME-5510L-XX	
VMIVME-5510L-xx:	Includes two VMIVME-5510 Link boards and cable assemblies xx feet long
Standard Links:	VMIVME-5510L-05 VMIVME-5510L-10 VMIVME-5510L-25
For Nonstandard Links, Order:	Two VMIVME-5510 Link boards plus two cable assemblies (one shielded and one unshielded)
For a Single Board, Order:	VMIVME-5510
Connector Data	
Compatible Connector Strain Relief PC Board Connector	Panduit No. 120-964-435 Panduit No. 100-000-072 Panduit No. 120-964-053A
Note	
Panduit is also known as ITW/Pancon.	

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chassis is granted the link. The arbiter resolves simultaneous access from both chassis by forcing one of the chassis to terminate its transfer via BERR or DTACK (this is software-selectable). The user can select single cycle (default upon power-up/reset) or multicycle (burst) access to the link. In SINGLE CYCLE MODE, arbitration is performed every time an address in either chassis falls within that chassis' address window. In MULTICYCLE MODE, one chassis is allowed to perform transfers across the link without interruptions (that is, arbitration is not performed on every cycle). MULTICYCLE MODE is requested by writing to an on-board register.

Attention Interrupts: VMEbus interrupt signals are isolated (not repeated). Processors in each chassis may generate an attention interrupt in the other chassis via register access on the VMIVME-5510.

SPECIFICATIONS

- Supports 8-, 16-, and 32-bit bidirectional data transfers
- Supports 16-, 24-, and 32-bit bidirectional addressing
- Memory protected by user-selectable access window. When VMEbus access is within window, it is repeated across the cable.
- Base address and address modifier in repeated chassis are user selectable
- Meets VMEbus specification - Rev. C. (for fully loaded chassis)
- High threshold logic provides high-noise immunity for all control signals
- Simultaneous accesses can be handled three ways: BERR, interrupt, or status check after transfer(s)
- Software isolation control mode for unlinked operation (multiprocessing)
- Switch-controlled isolation for maintenance
- Bidirectional attention interrupts over the cable (level and vector are software selectable)
- Data strobe latency in burst mode (no VMEbus arbitration) is typically 731 ns for 25-foot cables
- Typical DTACK latency for a write is 170 ns (496 ns for read) with 25-foot cables
- Allows expansion to multiple backplanes in a star expansion configuration (refer to Figure 2.)
- Double Eurocard form factor

CYCLE TIME MEASUREMENTS

- Write cycle time (data strobes asserted to data strobes deasserted) averages 1.097 µs
- Read cycle time (data strobes asserted to data strobes deasserted) averages 1.584 µs
- Both read and write tests performed in burst mode using force CPU 29XB, Force RR2 memory board, and 25-foot cables.

VMEbus SPECIFICATIONS

VMEbus Rev. C.1 Compliance: Master/Slave
A32/A24/A16
D32/D16/D08/(O)/D08 (EO) UAT

PHYSICAL/ENVIRONMENTAL

Temperature Range: 0 to 55 ˚C, operating
-20 to 85 ˚C, storage

Relative Humidity Range: 20 to 80 percent, noncondensing

Cooling: Forced convection

Power Requirements: 5 V
6.24 A maximum at 25 °C

Connector Data: DIN format

MTBF: 48,640 hours (217F)

CABLE DATA

Quantity: Two each 64-conductor

Type: Flat cable with integral shield (ground plane with two drain wires) utilized for address and data (3 M Part No. 3353/64).

Twist-and-Flat (Belden VARI-TWIST) used for control signals.

Length: 25 ft maximum

TRADEMARKS

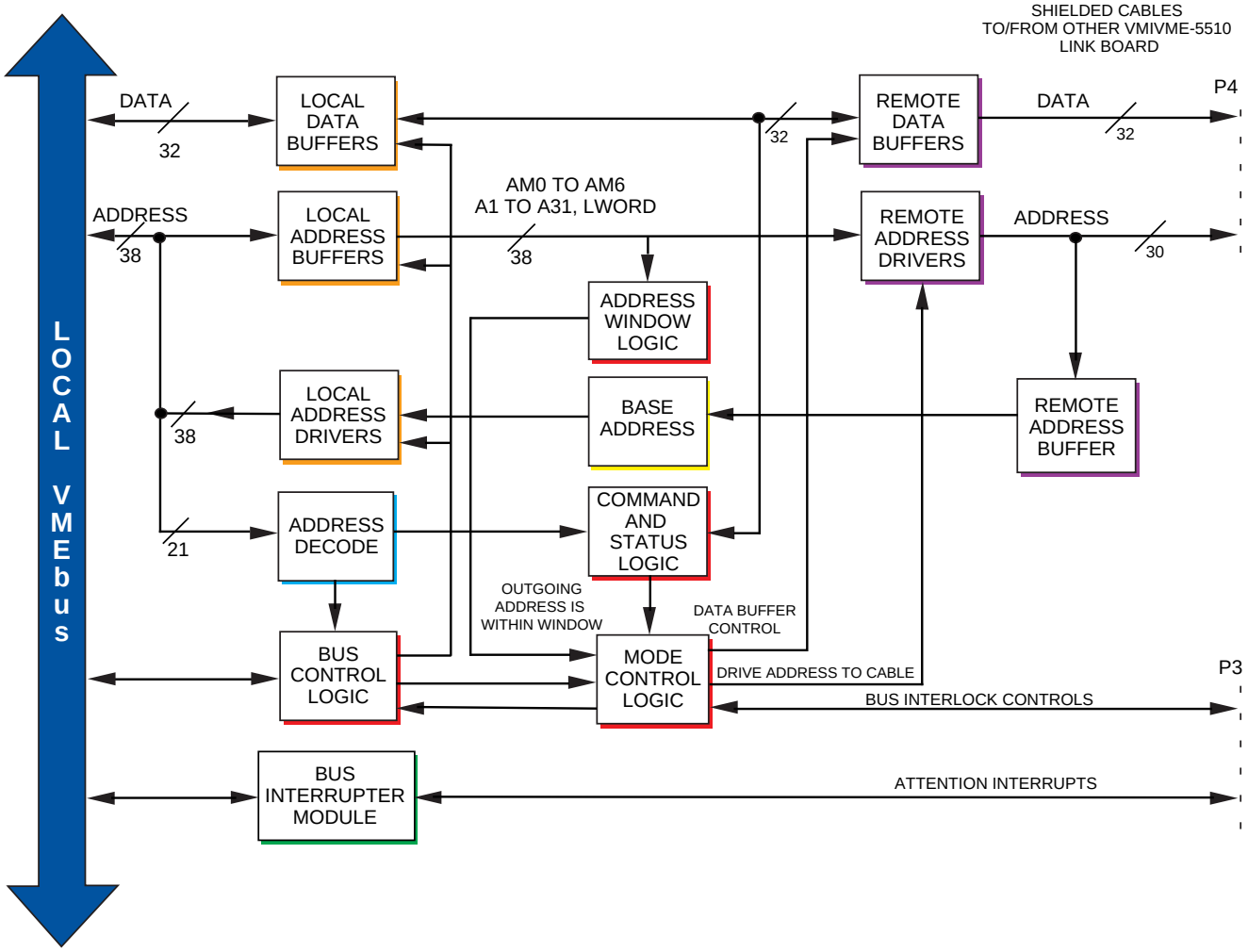

Figure 1. Functional Block Diagram of the VMIVME-5510 Multimaster Repeater Link Board

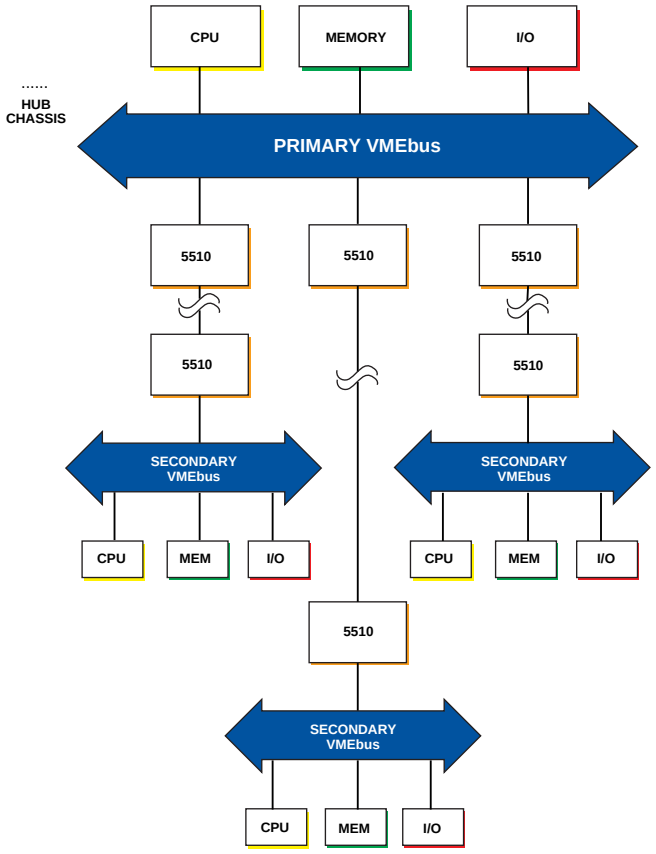

Figure 2. Star Configuration

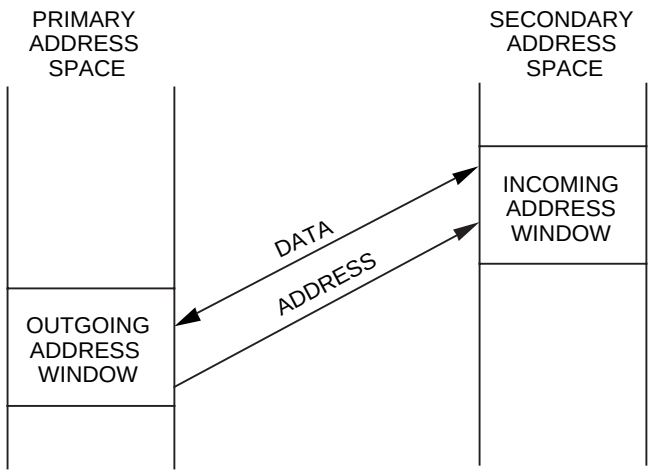

Figure 3. Software Transparent Mode

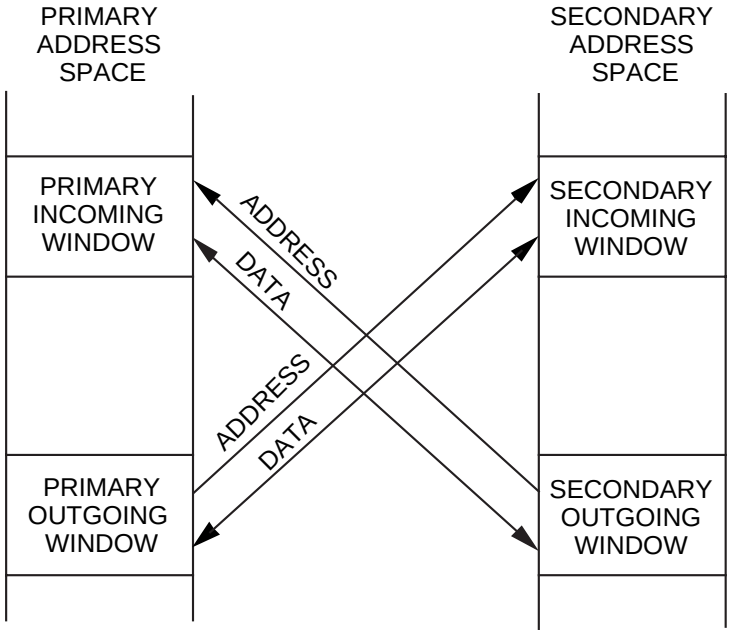

Figure 4. Multiprocessing Mode