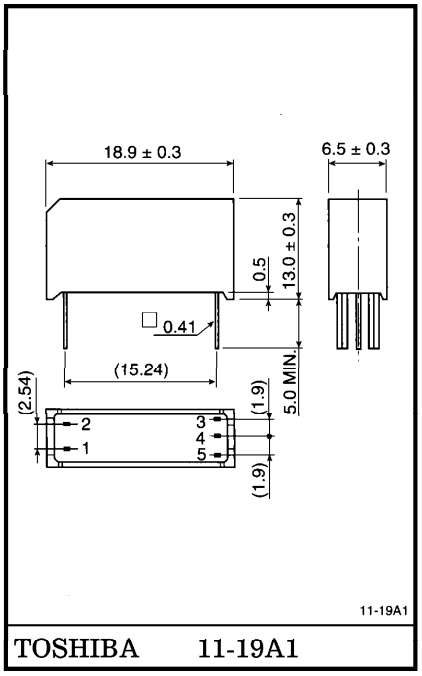
TOSHIBA PHOTOCOUPLER GaAℓAs IRED & PHOTO IC

TLP582

MOS FET GATE DRIVER

TRANSISTOR INVERTER

Unit in mm



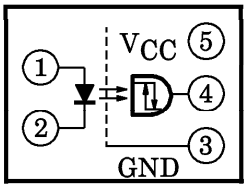
TOSHIBA 11-19A1

Weight : 1.55g

The TOSHIBA TLP582 consists of a GaAℓAs light emitting diode and integrated high gain, high speed photodetector.
The detector has a totem pole output circuit that provides source drive and sink drive, and built-in Schmitt trigger.
A fiber is used for light-coupling between LED and detector, and for sufficient separation between input side and output side.

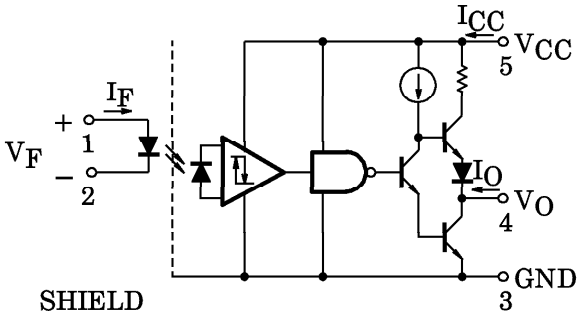
- Input Current : I_F = 5mA (MAX.)
- Power Supply Voltage : V_{CC} = 4.5~20V
- Switching Speed : t_{pHL}, t_{pLH} = 400ns (MAX.)
- Common Mode Transient Immunity : ±5000V / μs (MIN.)
- Guaranteed Performance Over Temperature : −25~85°C
- Isolation Voltage : 5000V_{rms} (MIN.)
- UL Recognized : UL1577, File No. E67349

PIN CONFIGURATION (TOP VIEW)



1 : LED ANODE
2 : LED CATHODE
3 : GND
4 : V_O (OUTPUT)
5 : V_{CC}

SCHEMATIC



A 0.1μF bypass capacitor must be connected between pins 3 and 5.

TRUTH TABLE (Positive Logic)

INPUT	OUTPUT
H	L
L	H

MAXIMUM RATINGS
(No Derating Required up to 85°C unless otherwise noted)

	CHARACTERISTIC		SYMBOL	RATING	UNIT
LED	Foward Current		I_F	25	mA
	Peak Transient Forward Current	(Note 1)	I_{FPT}	1	A
	Reverse Voltage		V_R	5	V
DETECTOR	Output Current		I_O	40 / −25	mA
	Peak Output Current	(Note 2)	I_{OP}	80 / −50	mA
	Output Voltage		V_O	−0.5~20	V
	Supply Voltage		V_{CC}	−0.5~20	V
	Output Power Dissipation	(Note 3)	P_O	100	mW
	Total Package Power Dissipation	(Note 4)	P_T	200	mW
Operating Temperature Range			T_{opr}	−40~85	°C
Storage Temperature Range			T_{stg}	−40~100	°C
Lead Solder Temperature (10s)			T_{sol}	260	°C
Isolation Voltage (AC, 1min., R.H.≦60%, Ta=25°C)		(Note 5)	BV_S	5000	V_{rms}

(Note 1) Pulse Width≦1μs, 300pps.
(Note 2) Pulse Width≦5μs, Duty Ratio≦0.025.
(Note 3) Derate 1.8mW / °C above 70°C ambient temperature.
(Note 4) Derate 3.6mW / °C above 70°C ambient temperature.
(Note 5) Device considered a two terminal device : pins 1, 2 shorted together, and pins 3, 4 and 5 shorted together.

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input Current, ON	$I_{F(ON)}$	7	8	20	mA
Input Voltage, OFF	$V_{F(OFF)}$	0	—	0.8	V
Supply Voltage	V_{CC}	4.5	—	20	V
Operating Temperature	T_{opr}	−25	—	85	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = −25~85°C、V_{CC} = 4.5~20V)

CHARACTERISTIC	SYMBOL	TEST CONDITION		MIN.	TYP.*	MAX.	UNIT
Input Forward Voltage	V_F	I_F = 5mA, Ta = 25°C		—	1.35	1.85	V
Temperature Coefficient of Forward Voltage	$\Delta V_F / \Delta Ta$	I_F = 5mA		—	−2	—	mV / °C
Input Reverse Current	I_R	V_R = 3V, Ta = 25°C		—	—	100	μA
Input Capacitance	C_T	V_F = 0, f = 1MHz, Ta = 25°C		—	170	—	pF
Output Leakage Current ($V_O > V_{CC}$)	I_{OHH}	V_F = 0V, V_{CC} = 4.5V	V_O = 5.5V	—	—	100	μA
			V_O = 20V	—	0.01	500	
Logic Low Output Voltage	V_{OL}	I_{OL} = 6.4mA, I_F = 5mA		—	0.4	0.5	V
Logic High Output Voltage	V_{OH}	I_{OH} = −2.6mA, V_F = 0.8V		2.4	3.3	—	V
Logic Low Supply Current	I_{CCL}	I_F = 7.5mA	V_{CC} = 5.5V	—	4.0	6.0	mA
			V_{CC} = 20V	—	4.6	7.5	
Logic High Supply Current	I_{CCH}	V_F = 0V	V_{CC} = 5.5V	—	4.2	6.0	mA
			V_{CC} = 20V	—	4.7	7.5	
Logic Low Short Circuit Output Current (Note 6)	I_{OSL}	I_F = 7.5mA	$V_O = V_{CC}$ = 5.5V	25	55	—	mA
			$V_O = V_{CC}$ = 20V	40	80	—	
Logic High Short Circuit Output Current (Note 6)	I_{OSH}	V_F = 0V, V_O = GND	V_{CC} = 5.5V	−10	−25	—	mA
			V_{CC} = 20V	−25	−60	—	
Input Current Logic Low Output	I_{FL}	I_O = 6.4mA, V_O < 0.4V		—	—	5	mA
Input Voltage Logic High Output	V_{FH}	I_O = −2.6mA, V_O > 2.4V		0.8	—	—	V
Input Current Hysteresis	I_{HYS}	V_{CC} = 5V		—	0.05	—	mA
Resistance (Input-Output)	R_S	V_S = 500V, R.H. ≦ 60%, Ta = 25°C (Note 5)		5×10^{10}	10^{14}	—	Ω
Capacitance (Input-Output)	C_S	V_S = 0, f = 1MHz, Ta = 25°C (Note 5)		—	0.15	0.3	pF

* All typical values are at Ta = 25°C, V_{CC} = 5V, IF (ON) = 7.5mA unless otherwise specified.

SWITCHING CHARACTERISTICS (Unless Otherwise specified, V_{CC} = 4.5~20V, Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.*	MAX.	UNIT
Propagation Delay Time to Logic High Output (Note 7)	t_{pLH}	1	I_F = 7.5→0mA	—	250	400	ns
Propagation Delay Time to Logic Low Output (Note 7)	t_{pHL}		I_F = 0→7.5mA	—	270	400	ns
Output Rise Time (10-90%)	t_r		I_F = 7.5→0mA, V_{CC} = 5V	—	35	75	ns
Output Fall Time (90-10%)	t_f		I_F = 0→7.5mA, V_{CC} = 5V	—	20	75	ns
Common Mode Transient Immunity at Logic High Output (Note 8)	C_{MH}	2	I_F = 0mA, V_{CM} = 400V V_O (Min.) = 2V	5	10	—	kV / μs
Common Mode Transient Immunity at Logic Low Output (Note 8)	C_{ML}		I_F = 7.5mA, V_{CM} = 400V V_O (Max.) = 0.8V	−5	−10	—	kV / μs

* All typical values are at Ta = 25°C, V_{CC} = 5V

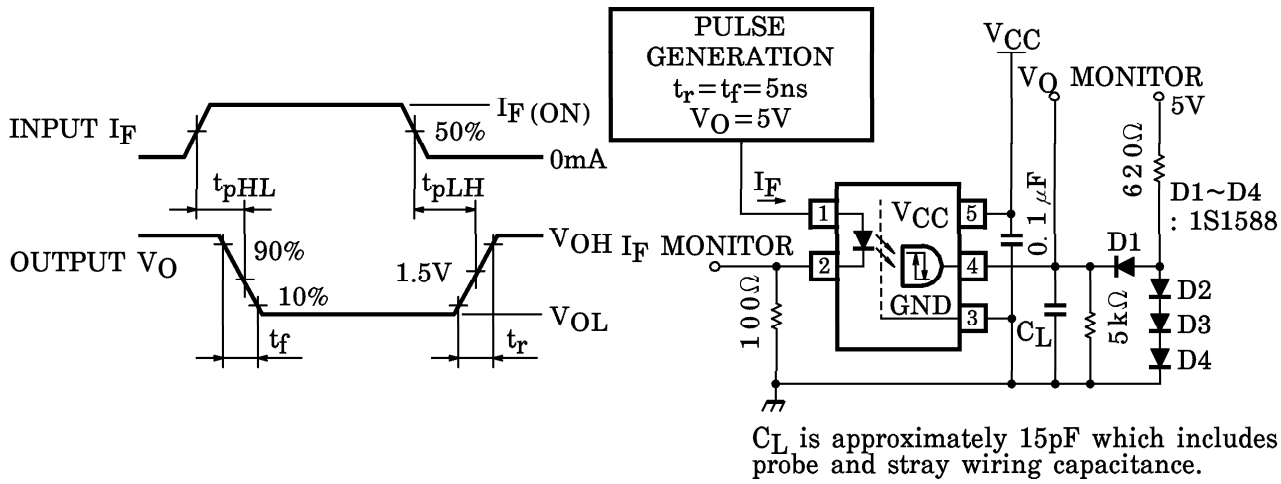
(Note 6) Duration of output short circuit time should not exceed 10ms.

(Note 7) The t_{pLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.5V point on the leading edge of the output pulse. The t_{pHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.

(Note 8) C_{ML} is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 0.8V). C_{MH} is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 2.0V).

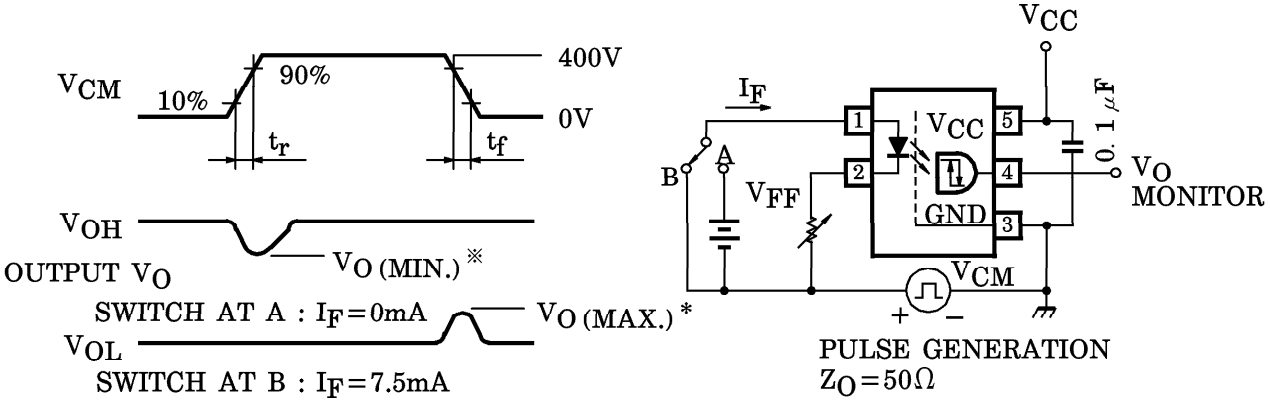
(Note 9) A ceramic capacitor (0.1μF) should be connected from pin 3 to pin 5 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1cm.

TEST CIRCUIT 1 : t_{pLH}, t_{pHL}, t_r and t_f



C_L is approximately 15pF which includes probe and stray wiring capacitance.

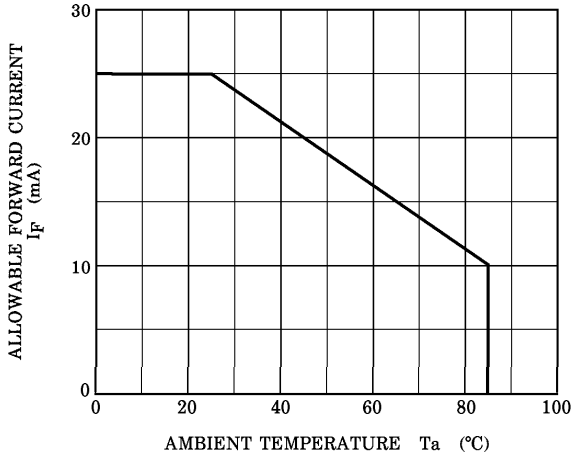
TEST CIRCUIT 2 : Common Mode Transient Immunity



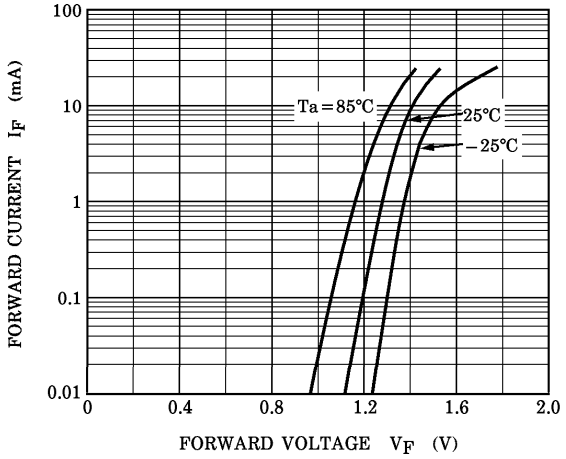
* SEE NOTE 8

$$C_{MH} = \frac{320\,(V)}{t_r\,(\mu s)},\ C_{ML} = \frac{320\,(V)}{t_f\,(\mu s)}$$

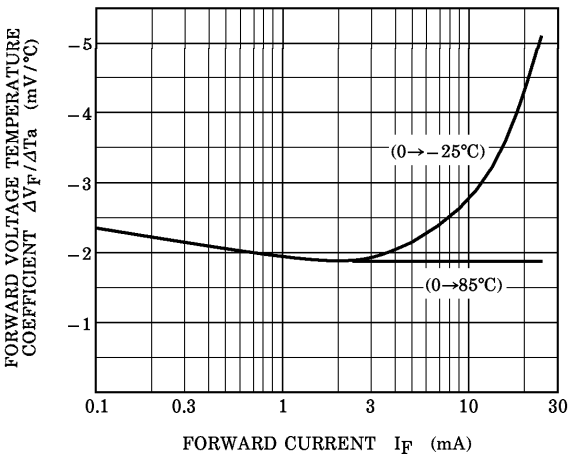
I_F – Ta



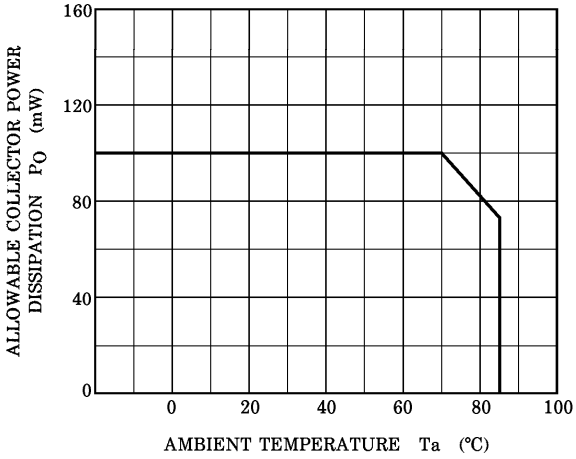
I_F – V_F



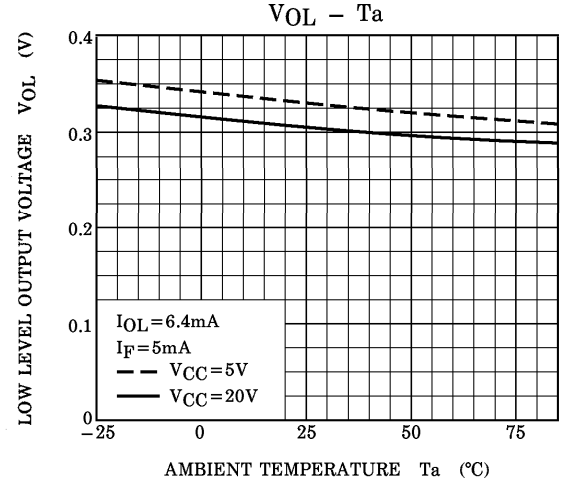
$\Delta V_F / \Delta Ta$ – I_F



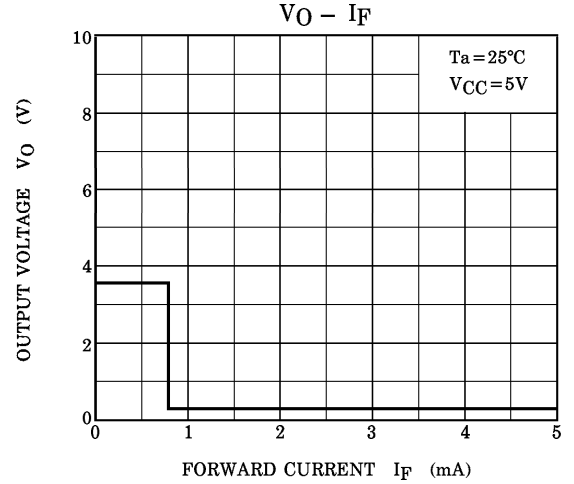
P_O – Ta



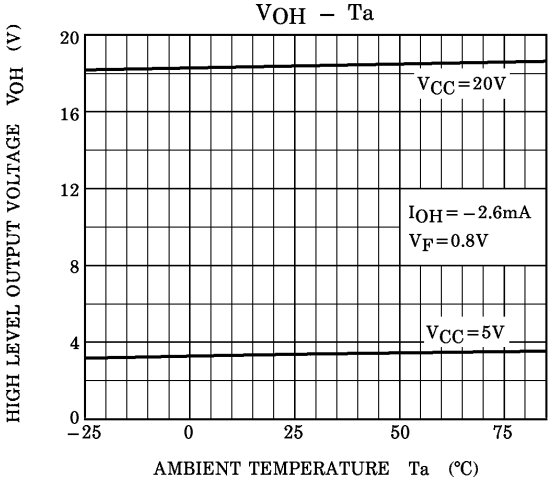
V_{OL} – Ta



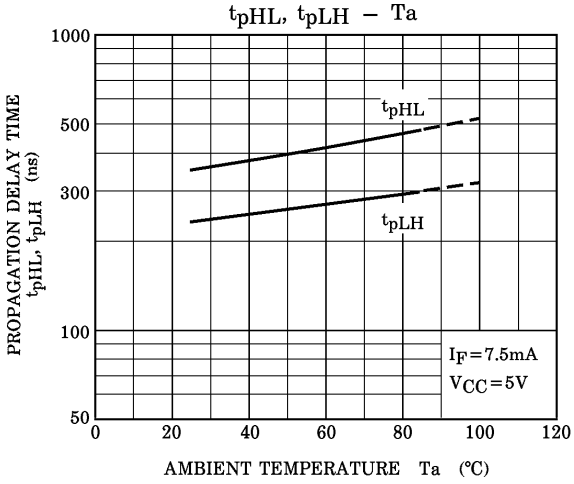
V_O – I_F



V_{OH} – Ta



t_{pHL}, t_{pLH} – Ta



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