TS-PMC A40 & A30

High Performance Video and Signal Processing

FPGA COMPUTING

Features

- Ideal for signal pre-processing, video, compression, software defined radio, radar, sonar and other high performance applications
- Micro-mezzanine I/O board allows for standard configuration and customization of I/O signals
- Micro-mezzanine connects to the front or rear panel interface for I/O flexibility
- User defined data can be routed through the P4 connection up to 1 Gigabytes/ sec
- Stratix® EP1S40 or EP1S30 FPGA delivers superior processing performance
- 1.8 Gigabyte per second combined memory bandwidth from two banks of SRAM and two banks of SDRAM
- 2 x 2Mbyte SRAM
- 2 x 128Mbyte SDRAM
- 64/ 66MHz PCI bus
- TS-Development Kits gets you up and running on an FPGA computing platform in less than an hour!
- Wave FPGA Software Tool Kit provides API, drivers, memory controller, source code, application examples and more
- Software compatible with other TS-Series FPGA computing products

The TS-PMC A40 & A30 is an FPGA processor solution targeted at high performance military and commercial computing applications. The large Stratix FPGA and high bandwidth capability, make it ideal for video and image processing, software defined radio, radar, sonar as well as other high performance signal processing applications.

The TS-PMC module uses a micro-mezzanine I/O concept to support off-the-shelf as well as custom I/O requirements. The micro-mezzanine offers the flexibility of front or rear panel connections.

High bandwidth processing is critical to most FPGA-based applications. TS-PMC offers four high speed/ high capacity memory banks, which can be two SRAM or SDRAM. This memory configuration offers over 500Mbytes/ second of memory access speed per SRAM bank and 400Mbytes/ second per SDRAM bank - delivering an aggregate memory bandwidth of over 1.8 Gigabytes/ second.

The TS-PMC is also available in a powerful, easy-to-use development kit environment, including Wave FPGA Software Tool Kit from SBS and Altera®'s soft-core Nios® II evaluation edition processor, and SOPC Builder – giving developers full access to SBS's resources with minimum effort.

All TS-Series of FPGA processors operate in a common Wave software development environment for easy migration across standard platforms. Develop on a TS-PCI and deploy it on a PMC!

The TS-PMC is one in a family of FPGA processors and I/O modules provided by SBS Technologies in many form factors including PCI, PCI-104 and CPCI.

TS-PMC A40 & A30

Specifications

Input/Output:

- Selectable 32 differential pairs between micro-mezzanine, P4 Rear Panel I/O and FPGA
- 64 bit/ 66MHz PCI bus between PMC connection and FPGA Local bus
- 32 bit/ 50 MHz PCI local bus
- LVDS I/O Mezzanine
  - 16 LVDS Input
  - 16 LVDS Outputs
  - 68 pin SCSI 3 Connection front panel connection
- Video PMC Mezzanine
  - Two RS-170 Video Inputs
  - One RS-170 Video Output
  - P4 rear panel connection
- Single analogue input 8 bit 133 KHz typically for IRIG data input

Operating System Support:

- Windows® XP/ 2000, Linux™, Integrity consult manufacturer

FPGA Resources:

- Altera Stratix EP1S40
  41,250 LUTS per FPGA
  14 DSP Blocks per FPGA
- Altera Stratix EP1S30
  32,470 LUTS per FPGA
  12 DSP Blocks per FPGA

Memory Resources:

- Two x 2Mbyte ZBT SRAM
- Two x 128Mbyte SDRAM

Power Requirements:

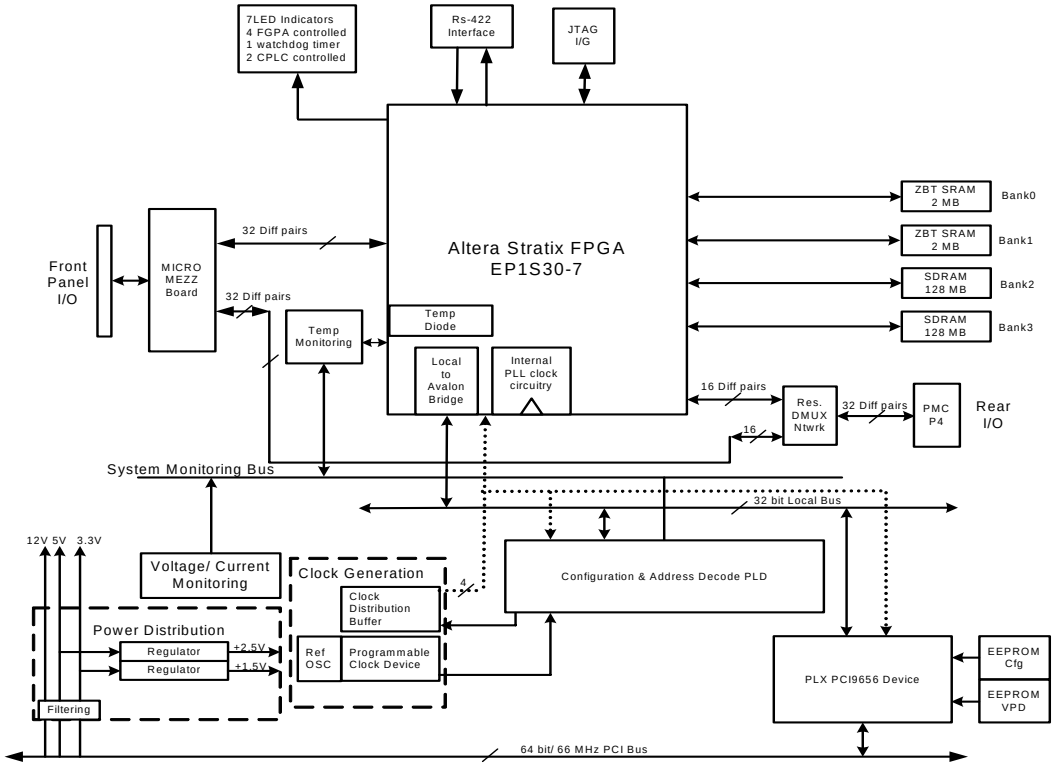
- 7.5 watts for typical PMC applications
- 12.5 Watts for PrPMC applications

Temperature:
Commercial Grade

- Operating: 0° to 55° C
- Storage: -45 ° to 85° C
- Humidity: 5% to 90%, non-condensing
- Air flow 100 LFPM

Conduction Cooled

Configuration



Ordering Information

Products

TS-PMC-3001	PMC, A30 Commercial Grade with EP1S30-C7 FPGA, 2 x 128MB SDRAM, 2 x 2MB SRAM, No Mezzanine I/O
TS-PMC-4001	PMC, A40 Commercial Grade with EP1S40-C5 FPGA, 2 x 128MB SDRAM, 2 x 2MB SRAM, No Mezzanine I/O
TS-PMC-4002	PMC, A40 Conduction Cooled with EP1S40-I6 FPGA, 2 x 128MB SDRAM, 2 x 2MB SRAM, No Mezzanine I/O
TS-IX-RS01	RS170 Video Mezzanine I/O for PMC with 2-RS170 input, 1 RS-170 output, rear panel I/O, conduction cooled compatible
TS-IX-RS02	RS-170 Conduction Cooled Micro-Mezzanine I/O for PMC 2-RS-170 input, 1 RS-170 output, rear panel I/O
TS-IX-LV01	LVDS Mezzanine I/O for PMC with 16 LVDS input, 16 LVDS output, SCSI3 front panel I/O
TS-IP-MP41	MPEG-4 encode algorithm optimized for the TS-PMC platform. See available datasheet for details

Development Kits

TS-DK-PMC03	PMC LVDS General Purpose Development Kit with TS-PMC-4001, TS-IX-LV01, Wave Software, Altera Quartus® II, Nios II evaluation edition and SOPC Builder
TS-DK-PMC02	PMC Video Development Kit with TS-PMC-4001, TS-IX-RS01, Wave Software, Altera Quartus II, Nios II evaluation edition and SOPC Builder

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