AR-B1423
INDUSTRIAL GRADE
CPU BOARD
User’ s Guide

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0. PREFACE

0.1COPYRIGHT NOTICE AND DISCLAIMER

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ACKNOWLEDGEMENTS

0.2 WELCOME TO THE AR-B1423 CPU BOARD

This guide introduces the Acrosser AR-B1423 CPU board.

The information provided in this manual describes about the card functions and features. It also helps you start, set up and operate your AR-B1423. General system information can also be found in this publication.

0.3 BEFORE YOU USE THIS GUIDE

Please refer to the Chapter 3, "Setting Up The System" in this guide, if you have not already installed this AR-B1423. Check the packing list before you install and make sure the accessories are completely included.

The AR-B1423 CD provides the newest information about the card**. Please refer to the files of the enclosed utility CD**. It contains the modification, hardware & software information. And it also has updated the product functions that may not be mentioned here.

0.4 RETURNING YOUR BOARD FOR SERVICE

If your board requires any services, contact the distributor or sales representative from whom you purchased the product for service information. If you need to ship your board to us for service, be sure it is packed in a protective carton. We recommend that you keep the original packaging for this purpose.

You can assure efficient servicing for your product by following these guidelines:

1. Include your name, address, daytime telephone and facsimile numbers and E-mail.
2. A description of the system configuration and/or software at the time is malfunction,
3. A brief description of the problem occurred.

0.5 TECHNICAL SUPPORT AND USER COMMENTS

User's comments are always welcome as they assist us in improving the quality of our products and the readability of our publications. They create a very important part of the input used for product enhancement and revision.

We may use and distribute any of the information you provide in anyway appropriate without incurring any obligation. You may, of course, continue to use the information you provide.

If you have any suggestions for improving particular sections or if you find any errors on it, please send your comments to Acrosser Technology Co., Ltd. or your local sales representative and indicate the manual title and book number.

Internet electronic mail to: **webmaster@acrosser.com**

Check our FAQ sheet for quick fixes to known technical problems.

0.6 ORGANIZATION

This manual covers the following topics (see the Table of Contents for a detailed listing):

- Chapter 1, "Overview", provides an overview of the system features and packing list.
- Chapter 2, "System Controller" describes the major structure.
- Chapter 3, "Setting Up the System", describes how to adjust the jumper, and the connector's settings.
- Chapter 4, "Installation", describes setup procedures including information on the utility diskette.
- Chapter 5, "BIOS Console", provides the BIOS options settings.

0.7 STATIC ELECTRICITY PRECAUTIONS

Before removing the board from its anti-static bag, read this section about static electricity precautions.

Static electricity is a constant danger to computer systems. The charge that can build up in your body may be more than sufficient to damage integrated circuits on any PC board. Therefore, it is very important to observe basic precautions whenever you use or handle computer components. Although areas with humid climates are much less prone to static build-up, it is always best to safeguard against accidents that may result in expensive repairs. The following measures should be sufficient to protect your equipment from static discharge:

- Touch a grounded metal object to discharge the static electricity in your body (or ideally, wear a grounded wrist strap).
- When unpacking and handling the board or other system components, place all materials on an anti-static surface.
- Be careful not to touch the components on the board, especially the "golden finger" connectors on the bottom of the board.

1. OVERVIEW

AR-B1423 Is a Consumer II /Elite PC-133 CPU Board with Ethernet, DOC, and Compact Flash (option).
This chapter provides an overview of your system features and capabilities. The following topics are covered:

- Specification
- Packing List
- Features
- Point for attention

1.1SPECIFICATION

- CPU: Consumer II/Elite PC-133 BGA.
- RAM Memory: one SO-DIMM socket.
- SSD: Support one socket for Disk On Chip.
- Watchdog: Software programmable 1~63sec.
- VGA Memory: AR-B1423 A -- UMA, shared system memory up to 4MB
  Supports CRT interface.
  AR-B1423B – Embedded 2MB SDRAM Video memory
  Supports CRT interface.
- VGA Interface: AR-B1423A – CRT-D-SUB 15pin female connector at bracket.
  AR-B1423B– CRT-D-SUB 15pin female connector at bracket.
  LCD with 2.0mm 44-pin Header connector.
- Ethernet: RTL82559ER chipset, supports ***10/100M baseT*** with RJ-45 connector
- Super I/O: Winbond 83977F-A
  1 EIDE (Ultra DMA33)– with one 2.0 mm 44-pin connector
  1 FDC – with 2.0 mm 34-pin connector.
  1 Parallel – with 2.54 mm 26-pin connector (supports SPP/EPP/ECP mode).
  1 ***RS-232C/RS485*** –COM1 Share with 485
  1 RS-232C /Touch Screen – with 2.0 mm 10-pin connector
  RS-232C is selectable by jumper and use the same connector.
  Touch Screen with 2.0mm 3-pin JST connector.
- BIOS: Flash BIOS AMI.
- Keyboard/Mouse: PS/2 compatible 6-pin mini-DIN connector.
- RTC: Chipset including, Support ***ACPI function*** with 7 years data retention.
- Expansion Bus: PC/104.
- Power Connector: One 4-pin Wafer Connector.
- Power Req.: +5V-2A maximum and 12V –0.01A maximum.
- PC Board: 10 layers, EMI considered
- Dimensions: 90.2mm x 95.9mm (3.5" X 3.7")

1.2 PACKING LIST

Some accessories are included with the system. Before AR-B1423 has been installed, please take a moment to make sure that the following items have been included inside the AR-B1423 package.

- The quick setup manual
- AR-B1423 CPU board
- Hard disk drive adapter cable for 2.5" HDD
- Floppy disk drive adapter cable.
- 4-in-1 adapter cable for COM1/COM2, parallel, and VGA
- PS/2 Y-type cable
- Ethernet adapter cable
- Power cable
- Software utility CD
- Screw kit

1.3 FEATURES

The system provides a number of special features that enhance its reliability, ensure its long-term availability, and improve its expansion capabilities, as well as its hardware structure.

- Consumer II/Elite PC-133 BGA
- One SO-DIMM socket.
- Supports DOC Flash Disk.
- 10/100M-Base Ethernet.
- Compact Flash (AR-B9462A) optional.
- AMI BIOS.
- Power Req.: +5V-1.4A maximum and 12V –0.01A maximum.
- 90.2mm x 95.9mm (3.5" X 3.7")

1.4 POINT FOR ATTENTION DIMENSIONS

The AR-B1423A CPU is a consumer II with C4 as a version that included some bugs on it. The effect is the use of floppy in WIN95 would be unable. The bug can be revised in CPU with C5 as a version. But according to ST as the original manufacturer, C5 just can normally be produced at least in October. The bug still exists so it is better to use the C4. Therefore, we decided to adopt no support as our temporary strategy.

In AR-B1423B section, we have to install WIN 95, and then set up the Floppy driver as the additional step in order to drive the AR-B1423B Floppy device properly.

The AR-B1423A& AR-B1423B can access from 64MB to 128MB of external memory.

2. SYSTEM CONTROLLER

This chapter describes the main structure of the AR-B1423 CPU board. The following topics are covered:

- Powerful x86 Processor
- 64-Bit SDRAM UMA Controller
- CRT Controller
- 2D Graphics Engine
- Interrupt Controller
- DMA Controller
- Timer/Counters
- IDE Controller
- Optional 16-Bit Local Bus Interface
- ISA Master/Slave
- PCI Master/Slave/Arbiter

2.1 POWERFUL X86 PROCESSOR

The AR-B1423 uses the Consumer II/Elite PC-133 BGA, it is an advanced 64-bit x86 processor block compatible processor offering high performance, fully accelerated 2D graphics, a 64-synchronous DRAM controller, all on a single chip. It includes a 64-bit SDRAM controller, a high speed PCI local-bus controller and Industry standard PC chip set functions (Interrupt controller, DMA Controller, Interval timer and ISA BUS).

- Fully static 32-bit five-stage pipeline, x86 processor fully PC compatible.
- Can access up to 128M of external memory.
- 8K byte unified instruction and data cache with write back and write through capability.
- Parallel processing integral floating-point unit, with automatic power down.
- Runs up to 133 MHz (x2)
- Fully static design for dynamic clock control.
- Low power and system management modes.
- Optimized design for 2.5 V operations.

2.2 64-BIT SDRAM UMA CONTROLLER

- 64-bit data bus.
- Up to100 MHz SDRAM clock speed.
- Integrated system memory, graphic frame memory and video frame memory.
- Supports 2MB up to 128 MB system memory
- Supports 16-, 64-, and 128-Mbit SDRAMs.
- Supports 8, 16, 32, 64, and 128 MB DIMMs.
- Supports buffered, non-buffered, and registered DIMMs.
- Four-line write buffers for CPU to SDRAM and PCI to SDRAM cycles.
- Four0line read pre-fetch buffers for PCI masters.
- Programmable latency
- Programmable timing for SDRAM parameters.
- Supports –8, -10, -12, -13, -15 memory parts.
- Supports memory hole between 1 MB and 8 MB for PCI/ISA busses.

The SDRAM controller only supports 64 bit wide Memory Banks.

Four Memory Banks (if DIMMS are used; Single sided or two doubled-sided DIMMs) are supported in the following configurations.

Memory Bank size	Number	Organization	Device Size
1Mx64	4	1Mx16	16Mbits
2Mx64	8	2Mx8	
4Mx64	16	4Mx4	
4Mx64	4	2Mx16x2	64Mbits
8Mx64	8	4Mx8x2	
16xM64	16	8Nx4x2	
4Mx64	4	1Mx16x4	
8Mx64	8	2Mx8x4	
32Mx64	16	4Mx4x4	
16Mx64	8	2Mx16x2	128Mbits
32Mx64	16	4Mx8x4	

Memory configurations

The SDRAM Controller supports buffered or unbuffered SDRAM but not EDO or FPM modes. SDRAMs must support Full Page Mode Type access.

The STPC Memory Controller provides various programmable SDRAM parameters to allow the SDRAM interface to be optimized for different processor bus speeds SDRAM grades and CAS Latency

This chapter defines the STPC Consumer-II Strap Options and their location. Some strap options are left programmable for future versions of silicon.

Strap Options

Signal	Designation	Actual Settings[1]	Set to '0'	Set to '1'
MD1	Reserved	Pull up	-	-
MD2	HCLK PLL Speed	User defined	see Section 3.1.4. bit 6	
MD3		User defined	see Section 3.1.4. bit 7	
MD4	PCICLKO Division	User defined	see Section 3.1.3. bit 1	
MD5	MCLK/HCLK Sync (see Section 3.1.1.)	User defined	Async	Sync
MD6	PCICLKO frequency	User defined	see Section 3.1.1. bit 6	
MD7	Reserved	Pull down	-	-
MD10	Reserved	Pull down	-	-
MD11	Reserved	Pull down	-	-
MD14	Reserved	Pull up	-	-
MD16	Reserved	Pull up	-	-
MD17	PCI_CLKO Divisor	User defined	see Section 3.1.3. bit 1	
MD18	Reserved	Pull-up	-	-
MD19	Reserved	Pull-up	-	-
MD20	DCLK Pad Direction	User defined	Input	Output
MD21	Reserved	Pull up	-	-
MD22	Reserved	Pull up	-	-
MD23	Reserved	Pull up	-	-
MD24	HCLK PLL Speed	User defined	see Section 3.1.4. bit 3	
MD25		User defined	see Section 3.1.4. bit 4	
MD26		User defined	see Section 3.1.4. bit 5	
MD27	Reserved	Pull down	-	-
MD28	Reserved	Pull down	-	-
MD29	Reserved	Pull down	-	-
MD30	Reserved	Pull down	-	-
MD40	CPU Mode (see Section 3.1.3.)	User defined	X1	X2
MD41	Reserved	Pull down	-	-
MD42	Reserved	Pull up	-	-
MD43	Reserved	Pull down	-	-
MD44	Bus select (see Section 3.1.1.)	User defined	ISA	Local Bus
MD45	Reserved	Pull down	-	-
MD46	Reserved	Pull up	-	-
MD47	Reserved	Pull down	-	-
MD48	Reserved	Pull up	-	-
TC	Reserved	Pull up	-	-
DACK_ENC[2:0]	Reserved	Pull up	-	-

Note[1]: Where a strap is represented by a 'Pull up' or 'Pull down', these have to be adhered to. If it is represented as a '-' it can be left unconnected. Where 'User defined', the strap is set by the user.

2.3 CRT CONTROLLER

- AR-B1423A Integrated 135 MHz triple RAMDAC allowing for 1024 x768 75 Hz displays.
- Requires external frequency synthesizer and reference sources.
- 8-bit, 16-bit, 24-bit pixels.
- Interlaced or non-interlaced output.
- Requires no external frequency synthesizer.
- Requires only external reference source.

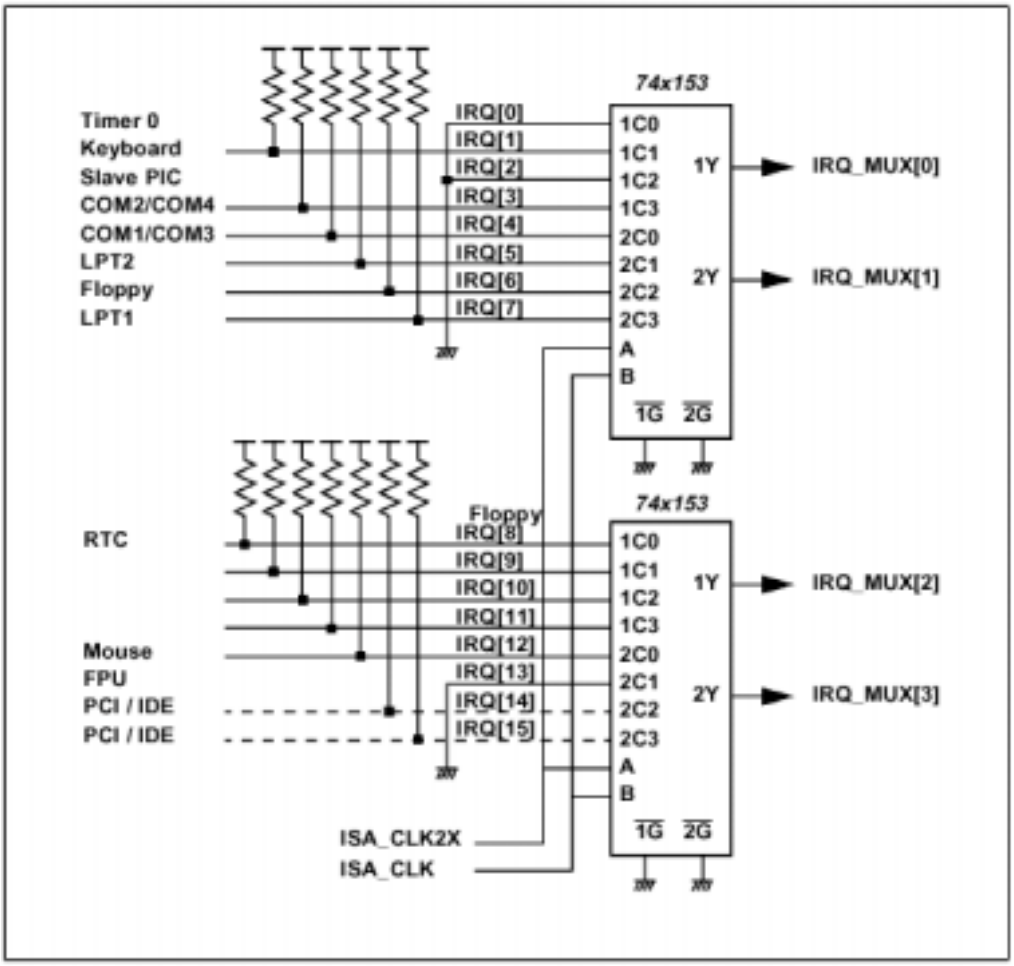
* **AR-B1423B has a special VGA controller C&T69000 supported CRT and LCD.**

2.4 2D GRAPHICS ENGINE

- 64-bit windows accelerator.
- Backward compatibility to SVGA standards.
- Hardware acceleration for text, bitblts, transparent blts and fills
- Up to 64 x 64 graphics hardware cursor.
- Up to 4MB long linear frame buffer.
- 8-bit, 16-bit and 24-bit pixels.
- Drivers available for various OSes.

2.5 INTERRUPT CONTROLLER

Most of the IPC signals are multiplexed: Interrupt inputs, DMA Request inputs, DMA Acknowledge outputs. The figure below describes a complete implementation of the IRQ [15:0] time multiplexing. When an interrupts line is used internally, the corresponding input can be grounded. In most of the embedded designs, only few interrupts lines are necessary and the glue logic can be simplified.



Typical IRQ multiplexing

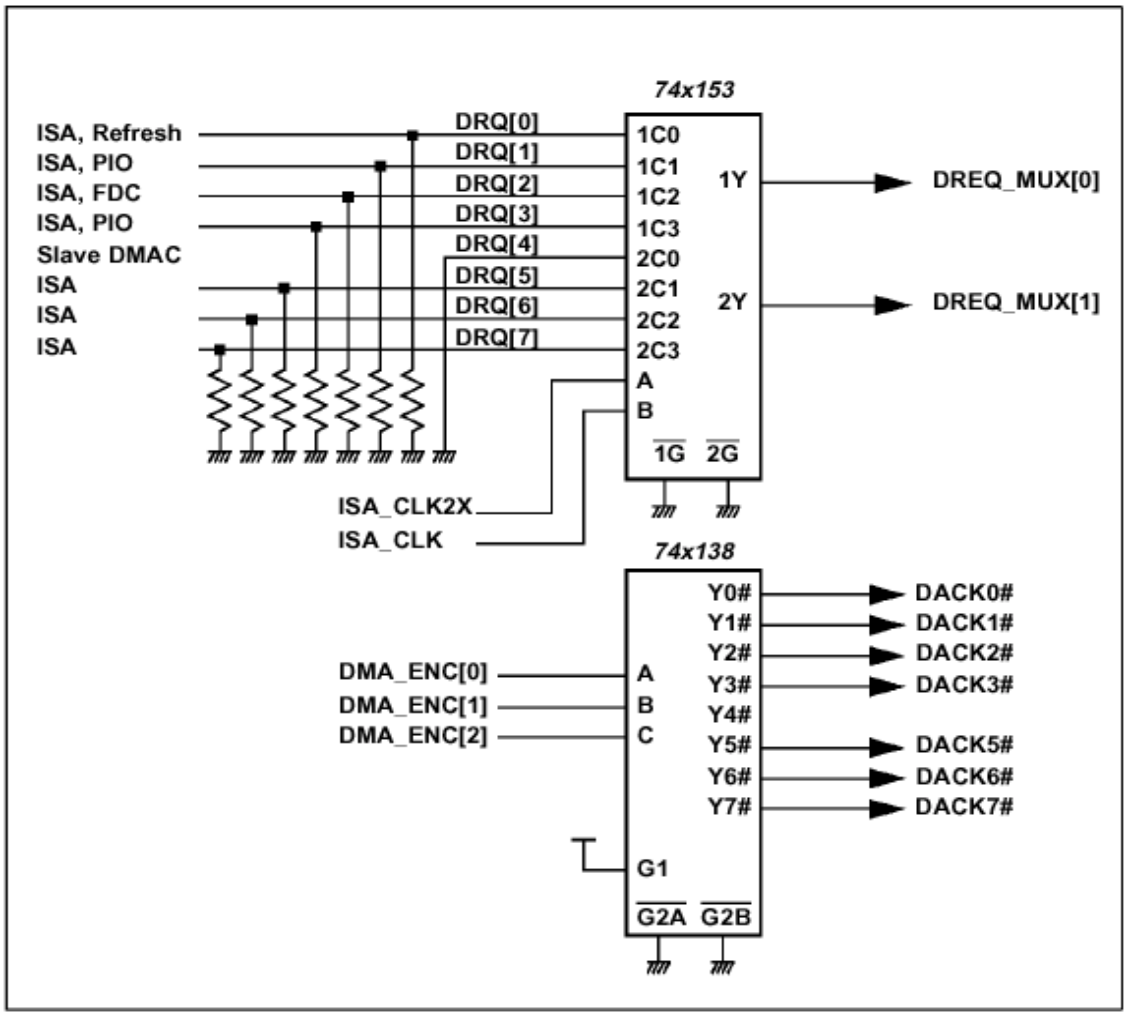
When the interface is integrated into the STPC, the corresponding interrupt line can be grounded as it is connected internally.

For example, if the integrated IDE controller is activated, the IRQ [14] and IRQ [15] inputs can be grounded.

2.6 DMA CONTROLLER

- **DMA channel**
- 2X8237/AT compatible 7-channel DMA controller integrated into the STPC.
- 2X8259/AT compatible interrupt Controller integrated into the STPC.
  16 interrupt inputs – ISA and PCI.
- Three 8254 compatible Timer/Counters integrated into the STPC.
- Co-processor error support logic.

The figure below describes a complete implementation of the external glue logic for DMA Request time-multiplexing and DMA Acknowledge demultiplexing. Like for the interrupt lines, this logic can be simplified when only few DMA channels are used in the application. This glue logic is not needed in Local bus mode and it does not support DMA transfers.



Typical DMA multiplexing and demultiplexing

2.7 TIMER / COUNTERS

- System Activity Detection.
- Three power down timers.
- Doze timer for detecting lack of system activity for short durations.
- Stand-by timer for detecting lack of system activity for medium durations.
- Suspend timer for detecting lack of system activity for long durations.
- Housekeeping activity detection.
- Housekeeping timer to cope with short bursts of housekeeping activity while dozing or in stand-by state.

2.8 IDE CONROLLER

- Supports PIO.
- Transfer Rates to 22 Mbytes/sec.
- Supports up to 2 IDE devices.
- Concurrent channel operation (PIO modes) –
  4 x 32-Bit Buffer FIFOs per channel.
- Support for PIO mode 3 & 4.
- Individual drive timing for all two IDE devices.
- Supports both legacy & native IDE modes.
- Supports hard drive larger than 528MB.
- Support for CD-ROM and tape peripherals.
- Backward compatibility with IDE (ATA-1).
- Drivers for Windows and other Operating Systems.

2.9 OPTIONAL 16-BIT LOCAL BUS INTERFACE

- Multiplexed with ISA/DMA interface.
- Low latency asynchronous bus.
- 22-bit address bus.
- 16-bit data bus with word steering capability.
- Programmable timing (Host clock granularity).
- Two Programmable Flash Chip Select.
- Four Programmable I/O Chip Select.
- Supports 32-bit Flash burst.
- Two-level hardware key protection for Flash boot block protection.
- Supports two banks of 16MB flash devices with boot block shadowed to 0x000F0000.

2.10 ISA MASTER / SLAVE

- Generates the ISA clock from either 14.318 MHz oscillator clock or PCI clock.
- Supports programmable extra wait state for ISA cycles.
- Supports I/O recovery time for back-to-back I/O cycles.
- Fast Gate A20 and Fast reset.
- Supports this single ROM that C, D, or E.
  Blocks shares with F block BIOS ROM.
- Supports flash ROM.
- Supports ISA hidden refresh.
- Buffered DMA & ISA master cycles to reduce bandwidth utilization of the PCI and Host bus.

2.11 PCI MASTER / SLAVE / ARBITER

- Fully compliant with PCI 2.1 specification.
- Integrated PCI arbitration interface. Up to 3 masters can connect directly. External PAL allows for greater then 3 masters.
- Translation of PCI cycles to ISA bus.
- Translation of ISA master initiated cycle to PCI
- Support for burst read/write from PCI master.
- PCI clock is 1/2, 1/3 or 1/4 CPU bus clock.

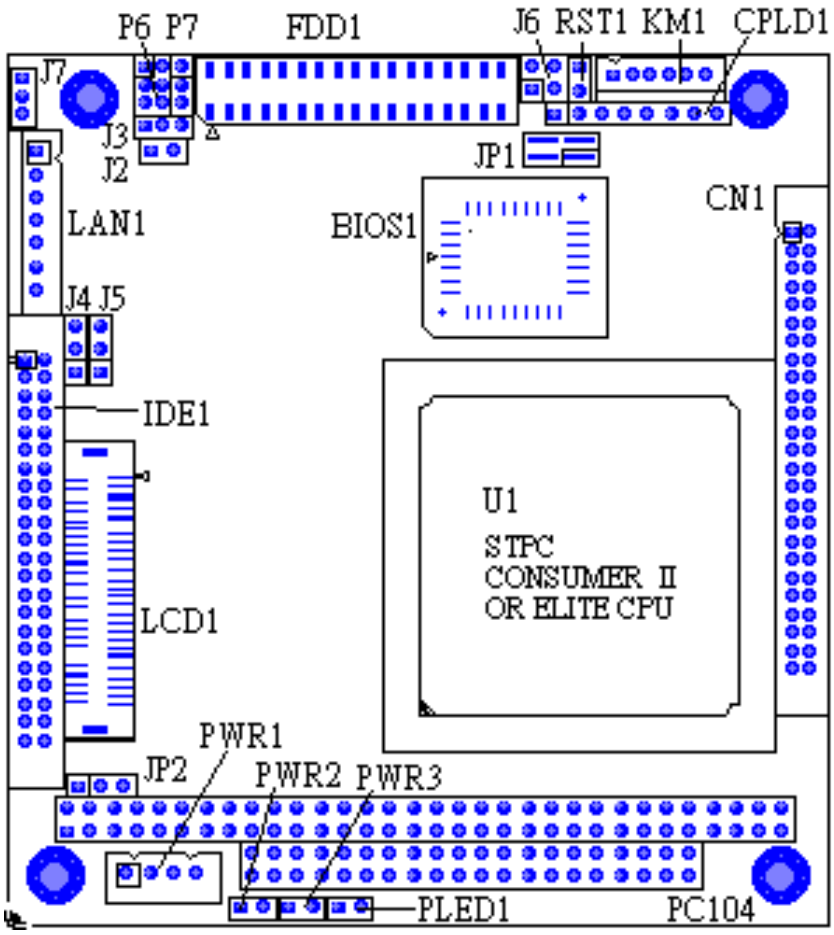
3. SETTING UP THE SYSTEM

This section describes pin assignments of on board connector and jumper settings.

- Overview
- System Setting

3.1 OVERVIEW

AR-B1423 is a 486 Grade CPU Board, which supports Ethernet, DOC, SSD, and Compact Flash (AR-B9462A) (option) functions. This section provides the hardware's jumper settings, the connectors' locations, and the pin assignments.



External System Location

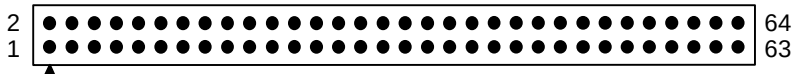
3.2 SYSTEM SETTING

Jumper pins allow you to set specific system parameters. Set them by changing the pin location of jumper blocks. (A jumper block is a small plastic-encased conductor that slips over the pins.) To change a jumper setting, remove the jumper from its current location with your fingers or small needle-nosed pliers. Place the jumper over the two pins designated for the desired setting. Press the jumper evenly onto the pins. Be careful not to bend the pins.

CAUTION: Do not touch any electronic components unless you are safely grounded. Wear a grounded wrist strap or touch an exposed metal part of the system unit chassis. The static discharges from your fingers can permanently damage electronic components.

3.2.1 PC/104 Connector

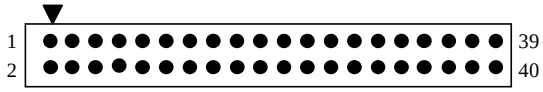
(1) 64 Pin PC/104 Connector Bus A & B (PC1)



64 Pin PC/104 Connector

PIN NO	SIGNAL	PIN NO	SIGNAL
1	–IOCHCK	2	GND
3	SD7	4	RSTDRV
5	SD6	6	VCC
7	SD5	8	IRQ9
9	SD4	10	Not Used
11	SD3	12	DREQ2
13	SD2	14	Not Used
15	SD1	16	–ZEROWS
17	SD0	18	(+12V)
19	IOCHRDY	20	GND
21	AEN	22	–SMEMW
23	SA19	24	–SMEMR
25	SA18	26	–IOW
27	SA17	28	–IOR
29	SA16	30	–DACK3
31	SA15	32	DREQ3
33	SA14	34	–DACK1
35	SA13	36	DREQ1
37	SA12	38	–REFRESH
39	SA11	40	SYSCLK
41	SA10	42	IRQ7
43	SA9	44	IRQ6
45	SA8	46	IRQ5
47	SA7	48	IRQ4
49	SA6	50	IRQ3
51	SA5	52	–DACK2
53	SA4	54	TC
55	SA3	56	BALE
57	SA2	58	VCC
59	SA1	60	OSC
61	SA0	62	GND
63	GND	64	GND

(2) 40 Pin PC/104 Connector Bus C & D (PC1)

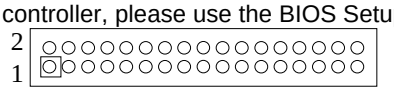


40 Pin PC/104 Connector

PIN NO	SIGNAL	PIN NO	SIGNAL
1	GND	2	GND
3	–SBHE	4	–MEMCS16
5	LA23	6	–IOCS16
7	LA22	8	IRQ10
9	LA21	10	IRQ11
11	LA20	12	IRQ12
13	LA19	14	IRQ15
15	LA18	16	IRQ14
17	LA17	18	–DACK0
19	–MEMR	20	DREQ0
21	–MEMW	22	–DACK5
23	SD8	24	DREQ5
25	SD9	26	–DACK6
27	SD10	28	DREQ6
29	SD11	30	–DACK7
31	SD12	32	DREQ7
33	SD13	34	VCC
35	SD14	36	–RMASTER
37	SD15	38	GND
39	Not Used	40	GND

3.2.2 FDD Port Connector (FDD1)

The AR-B1423 provides a 34-pin header type connector for supporting up to two floppy disk drives. To enable or disable the floppy disk controller, please use the BIOS Setup program.



FDD1: FDD Port connector

PIN NO	PIN DEFINITION	PIN NO	PIN DEFINITION
1	GND	2	DRVEN0
3	GND	4	NC
5	GND	6	DRVEN1
7	GND	8	INDEX#
9	GND	10	MOA#
11	GND	12	DSB#
13	GND	14	DSA#
15	GND	16	MOB#
17	GND	18	DIR#
19	GND	20	STEP#
21	GND	22	WD#
23	GND	24	WE#
25	GND	26	TRACK0#
27	GND	28	WP#
29	GND	30	RDATA#
31	GND	32	HEAD#
33	GND	34	DSKCHG#

FDD Pin Assignment

3.2.3 Mini-DIN Connector (LAN1)

The LAN1 Mini-DIN headers are the standard network headers. The following table is the pin assignment.

PIN (LAN1)	FUNCTION
1	RTX+
2	RTX-
3	NRX+
4	NRX-
5	Not Used
6	Not Used
7	Not Used

LAN1 Pin Assignment

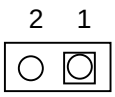
3.2.4 PS/2 Mouse & Keyboard Connector (KM1)

To use the PS/2 interface, an adapter cable has to be connected to the CN2 (6-pin header type) connector. This adapter cable is mounted on a bracket and is included in your AR-B1423 package. The connector for the PS/2 KB/mouse is a Mini-DIN 6-pin connector. Pin assignments for the PS/2 port connector are as follows:

PIN#	PIN DEFINITION
1	MOUSE DATA
2	KB DATA
3	GND
4	VCC
5	MOUSE CLOCK
6	KB CLOCK

3.2.5 Reset Header (RST1)

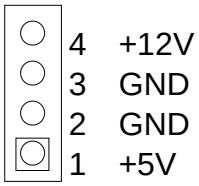
Shorting these two pins will reset the system



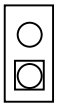
RST1

3.2.7 Power Connector (PWR1 & PWR2 & PWR3)

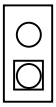
The PWR1 is a 4-pin power connector. PWR2 and PWR3 is 2-pin one. They are the standard connectors on all Acrosser boards.



PWR1

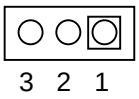


PWR2



PWR3

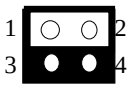
3.2.8 Touch Screen Connector (J4 & J5)



1. RXDF
2. TXDF
3. CGND

3.2.9 D.O.C. Memory Bank Address Select (JP1)

This section provides the information about how to use the D.O.C. (Disk On Chip). It divided into two parts: hardware setting and software configuration.



Factory Preset

JP1: D.O.C. Memory Address

JP1	Address	Note
1-2 3-4	D200:0000	
3-4	CC00:0000	
1-2	C800:0000	Factory Preset
X	D000:0000	

(Only for AR-B1423A)

JP1	Address	Note
1-2 3-4	D000:0000	
3-4	D200:0000	
1-2	D400:0000	Factory Preset
X	D600:0000	

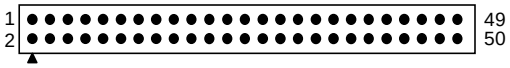
(Only for AR-B1423B)

Step 1: Use JP1 to select the correct D.O.C. memory bank address.

Step 2: Insert programmed Disk On Chip into sockets DOC1 setting as DOC.

Step 3: Line up and insert the AR-B1423A and AR-B1423B card into slot of your back plane.

3.2.10 Multi-Function Port Connector (CN1)

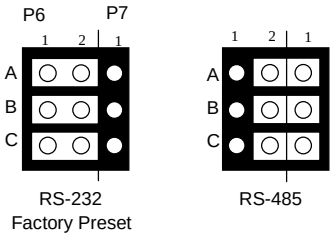


CN1 COM1/COM2, parallel, and VGA 4-in-1 Connector

PORT	PIN NO	SIGNAL	PIN NO	SIGNAL
COM1	1	DCD1	2	DSR1
	3	RXD1	4	RTS1
	5	TXD1	6	CTS1
	7	DTR1	8	RI1
	9	GROUND	10	CASE GND
COM2	11	DCD2	12	DSR2
	13	RXD2	14	RTS2
	15	TXD2	16	CTS2
	17	DTR2	18	RI2
	19	GROUND	20	GROUND
PARALLEL	21	STROBE	22	AUTO FORM FEED
	23	DATA 0	24	ERROR
	25	DATA 1	26	INITIALIZE
	27	DATA 2	28	PRINTED SELECT IN
	29	DATA 3	30	DATA 4
	31	DATA 5	32	DATA 6
	33	DATA 7	34	ACKNOWLEDGE
	35	BUSY	36	PAPER
	37	GROUND	38	PRINTER SELECT
	39	GROUND	40	GROUND
VGA	41	RED	42	VGA GROUND
	43	GREEN	44	GROUND
	45	BLUE	46	GROUND
	47	HORIZONTAL SYNC	48	DDC DATA
	49	VERTICAL SYNC	50	DDC CLOCK

(1) RS-232/RS-485 Select for COM1 (P6 & P7)

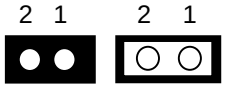
The P6 &P7 jumpers are designed for selecting the use of 0n-board RS-232 or RS-485 for the COM1



RS-232 Factory Preset　　RS-485

(2) RS-485 Terminator Select (J2)

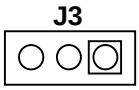
When there is only one line the setting should be left off (please take off the jumper), if multiple blocks are used on a single line this should be set to "ON"(place a jumper) in order to properly terminate the connection for better transmission.



OFF　　ON

Factory Preset

(3) RS-485 Header (J3)



1. N485+
2. N485-
3. GND

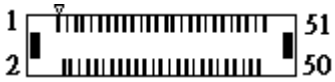
3.2.11 LCD Supported Voltage LCD1 Select (JP2)

(Only for AR-B1423B)

3.3V (Factory Preset)　　5V

3.2.12 LCD Panel Display Connector (LCD1)

(Only for AR-B1423B)



The pin assignment of LCD connector is shown below:

LCD1: LCD Display Connector

- The resolution can support CRT on 640*480
  800*600
  1024*768
  1280*1024
- The resolution can support LCD on 640*480
  800*600
  1024*768

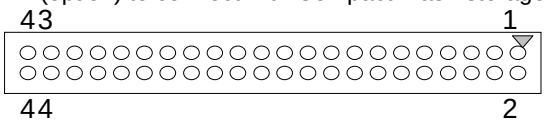
PIN	SIGNAL	PIN	SIGNAL
1	FP0	2	FP16
3	FP1	4	FP17
5	FP2	6	FP18
7	FP3	8	FP19
9	FP4	10	FP20
11	FP5	12	FP21
13	FP6	14	FP22
15	FP7	16	FP23
17	LCDVDD	18	LCDVDD
19	FP8	20	FP24
21	FP9	22	FP25
23	FP10	24	FP26
25	FP11	26	FP27
27	FP12	28	FP28
29	FP13	30	FP29
31	FP14	32	FP30
33	FP15	34	FP31
35	FP34	36	FP32
37	FP35	38	FP33
39	M/DE	40	GND
41	VCC	42	FLM
43	VCC	44	GND
45	ENABLK	46	SHFCLK
47	ENAVEE	48	GND
49	(+12V)	50	LP
51	(+12V)	52	

LCD Pin Assignment

3.2.13 Hard Disk (IDE1) Connector

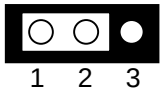
44-Pin Hard Disk Connector (IDE1)

AR-B1423 provides 44-pin connector (IDE1) interface to connect with the hard disk device. Furthermore, user could also apply AR-B9462A (option) to connect with Compact Flash storage device.

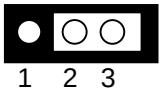


Pin #	Signal	Pin #	Signal
1	RESET	2	GROUND
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DATA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14
17	DATA 0	18	DATA 15
19	GROUND	20	NOT USED
21	IDEDREQ	22	GROUND
23	-IOW A	24	GROUND
25	-IOR A	26	GROUND
27	IDEIORDYA	28	GROUND
29	-DACKA	30	GROUND
31	AINT	32	GROUND
33	SA 1	34	Not Used
35	SA 0	36	SA 2
37	CS 0	38	CS 1
39	HDD LED	40	GROUND
41	VCC	42	VCC
43	GROUND	44	Not Used

1.14 Clear CMOS Jumper(J7)

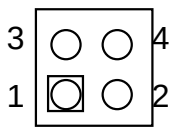


1-2:Normal(Factory Preset)



2-3:Clear

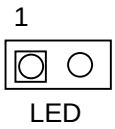
1.15 Hardisk LED Header (J6)



J6

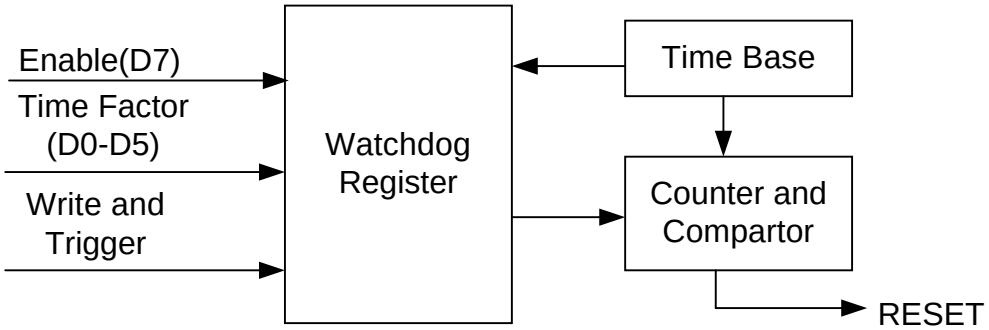
PIN NO	PIN DEFINITION
1	HLED+
2	HLED-
3	PWLED-
4	PWLED+

1.16 Power LED Header (PLED1)



3.3 WATCHDOG TIMER

This section describes the use of Watchdog Timer, including disable, enable, and trigger. AR-B1423 is equipped with a programmable time-out period watchdog timer that occupies I/O port 443H. Users can use simple program to enable the watchdog timer. Once you enable the watchdog timer, the program should trigger it every time before it times out. Watchdog Timer will generate a response (system or IRQ) due to system fails to trigger or disable watchdog timer before preset timer, times out.



Watchdog Block Diagram

3.3.1 Watchdog Timer Setting

The watchdog timer is a circuit that maybe be used from your program software to detect crash or hang up. The Watchdog timer is automatically disabled after reset. Once you enabled the watchdog timer, your program should trigger the watchdog timer every time before it times out. After you trigger the watchdog timer, the timer will be set to zero and start to count again. If your program fails to trigger the watchdog timer before times out, it will generate a reset pulse to reset the system or trigger the IRQ 9 signal in order to tell your system that the watchdog time is out.

Please refer to the following table in order to properly program Watchdog function

	D7	D6	D5 D4 D3 D2 D1 D0
1	Enable	Reset	Time period
0	Disable	IRQ 9	

Users could test watchdog function under 'Debug' program as follows:

C:>debug

- O 443 CFH
  Generally, watchdog function would reset system after 15 seconds
- O 443 40H
  Disable watchdog function

C:>debug
- O 443 88H
  Generally, watchdog function would generate IRQ 9 after 8 seconds
- O 443 40H
  Disable watchdog function

3.3.2 Watchdog Timer Trigger

After you enable the watchdog timer, your program must write the same factor as triggering to the watchdog timer at least once during every time-out period. You can change the time-out period by writing another timer factor to the watchdog register at any time, and you must trigger the watchdog during every new time-out period in next trigger.

C:>debug
- O 443 88H
  Generally, watchdog function would generate IRQ 9 after 8 seconds
- O 443 83H
  Disable last watchdog function. Watchdog function would Generate IRQ 9 after 3 seconds.

C:>debug
- O 443 CFH
  Generally, watchdog function would reset system after 15 seconds
- O 443 C3H
  Disable last watchdog function. Watchdog function would reset system after 3 seconds.

4. INSTALLATION

This chapter describes the installation procedure. The following topics are covered:

- Overview
- Utility CD

4.1 OVERVIEW

This chapter provides information for you to set up a working system based on the AR-B1423 CPU board. Please carefully read the details of the CPU board's hardware descriptions before installation. Pay special attention to the jumper settings, switch settings and cable connections.

Follow steps listed below for proper installation:

Step 1: Read the CPU board's hardware description in this manual.

Step 2: Set jumpers.

Step 3: Make sure that the power supply connected to your AR-B1423 CPU board is turned off.

Step 4: Connect all necessary cables. Make sure that the HDD; serial and parallel cables are connected to pin 1 of the related connector (not upside down).

Step 5: Connect the hard disk flat cables from the CPU board to the drives. Connect a power source to drive.

Step 6: Plug the keyboard into the keyboard connector.

Step 7: Turn on the power.

Step 8: Configure your system with the BIOS Setup program (section 5) then re-boot your system.

Step 9: If the CPU board does not work, turn off the power and read the hardware description carefully again.

Step 10: If the CPU board still does not perform properly, return the board to your dealer for immediate service.

4.2 UTILITY CD

The AR-B1423 provides a piece of which contains necessary drivers and utility for installing AR_B1423.

4.2.1 Driver Installation

Generally, the CD that comes with AR-B1423 should be able to carry out 'Auto run' function, please follows the instruction displayed on the screen to install drives. In case, if the 'Auto run' function is fail, please execute 'Setup.exe' program under root directory of the CD.

5. BIOS CONSOLE

This chapter describes the AR-B1423 BIOS menu displays and explains how to perform common tasks needed to get up and running, and presents detailed explanations of the elements found in each of the BIOS menus. The following topics are covered:

- BIOS Setup Overview
- Standard CMOS Setup
- Advanced CMOS Setup
- Advanced Chipset Setup
- Power Management Setup
- PCI/Plug and Play Setup
- Peripheral Setup
- Password Setting
- Load Default Setting
- BIOS Exit

5.1 BIOS SETUP OVERVIEW

The BIOS is a program used to initialize and set up the I/O system of the computer, which includes the ISA bus and connected devices such as the video display, diskette drive, and the keyboard.

The BIOS provides a menu-based interface to the console subsystem. The console subsystem contains special software, called firmware that interacts directly with the hardware components and facilitates interaction between the system hardware and the operating system.

The BIOS default values ensure that the system will function at its normal capability. In the worst situation the user may have corrupted the original settings set by the manufacturer.

After the computer is turned on, the BIOS will perform diagnostics on the system and display the size of the memory that is being tested. Press the [Del] key to enter the BIOS Setup program, and then the main menu will show on the screen.

The BIOS Setup main menu includes some options. Use the [Up/Down] arrow key to highlight the option that you wish to modify, and then press the [Enter] key to select the option and configure the functions.

Figure 5-1 BIOS: Setup Main Menu

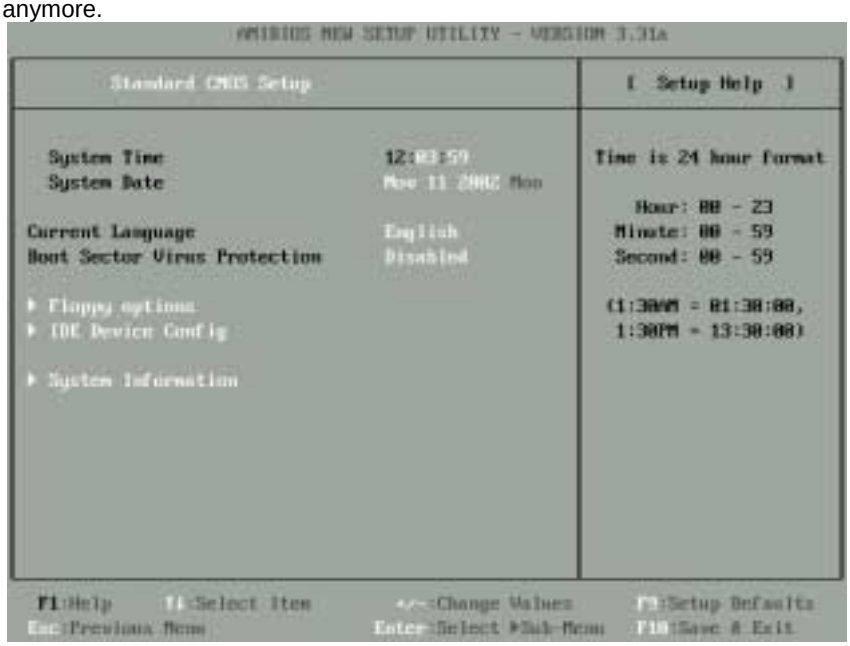
CAUTION: 1. AR-B1423 BIOS the factory-default setting is used to the <Auto Configuration with Optimal Settings> Acrosser recommends using the BIOS default setting, unless you are very familiar with the setting function, or you can contact the technical support engineer.

2. If the BIOS settings are lost, the CMOS will detect the <Auto Configuration with Fail Safe Settings> to boot the operation system, this option will reduce the performance of the system. Acrosser recommends choosing the <Auto Configuration with Optimal Setting> in the main menu. This option gives best-case values that should optimize system performance.

3. The BIOS settings are described in detail in this section.

5.2 STANDARD CMOS SETUP

The <Standard CMOS Setup> option allows you to record some basic system hardware configuration and set the system clock and error handling. If the CPU board is already installed in a working system, you will not need to select this option anymore.



Standard CMOS Setup

Date & Time Setup

Highlight the <Date> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the month, day and year format.

Highlight the <Time> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the hour, minute and second format.

The user can bypass the date and time prompts by creating an AUTOEXEC.BAT file. For information on how to create this file, please refer to the MS-DOS manual.

Hard Disk Setup

The BIOS supports various types for user settings, The BIOS supports <Pri Master>, <Pri Slave>, so the user can install up to two hard disks. For the master and slave jumpers, please refer to the hard disk's installation descriptions and the hard disk jumper settings in section three of this manual.

You can select <AUTO> under the <TYPE> and <MODE> fields. This will enable auto detection of your IDE drives during boot-up. This will allow you to change your hard drives (with the power off) and then power on without having to reconfigure your hard drive type. If you use older hard disk drives, which do not support this feature, then you must configure the hard disk drive in the standard method as described above by the <USER> option.

Floppy Setup

The <Standard CMOS Setup> option records the types of floppy disk drives installed in the system.

To enter the configuration value for a particular drive, highlight its corresponding field and then select the drive type using the left-or right-arrow key.

5.3 ADVANCED CMOS SETUP

The <Advanced CMOS Setup> option consists of configuration entries that allow you to improve your system performance, or let you set up some system features according to your preference. Some entries here are required by the CPU board's design to remain in their default settings.

Advanced CMOS Setup

Quick Boot

This category speeds up Power On Self Test (POST) after you power on the computer. If it is set to ***Enabled***, BIOS will shorten or skip some check items during POST.

1st Boot Device
2nd Boot Device
3rd Boot Device

These options determine where the system looks first for an operating system.

Boot Up Num-Lock

This item is used to activate the Num-Lock function upon system boot. If the setting is on, after a boot, the Num-Lock light is lit, and user can use the number key.

Floppy Drive Swap

The option reverses the drive letter assignments of your floppy disk drives in the Swap A, B setting, otherwise leave on the setting of ***Disabled*** (No Swap). This works separately from the BIOS Features floppy disk swap feature. It is functionally the same as physically interchanging the connectors of the floppy disk drives. When <***Enabled***>, the BIOS swapped floppy drive assignments so that Drive A becomes Drive B, and Drive B becomes Drive A under DOS.

Floppy Drive Seek

If the <Floppy Drive Seek> item is setting ***Enabled***, the BIOS will seek the floppy <A> drive one time upon boot up.

PS/2 Mouse Support

The setting of ***Enabled*** allows the system to detect a PS/2 mouse on boot up. If detected, IRQ12 will be used for the PS/2 mouse. IRQ 12 will be reserved for expansion cards if a PS/2 mouse is not detected. ***Disabled*** will reserve IRQ12 for expansion cards and therefore the PS/2 mouse will not function.

Typematic Rate

This item specifies the speed at which a keyboard keystroke is repeated.

System Keyboard

This function specifies that a keyboard is attached to the computer.

Primary Display

The option is used to set the type of video display card installed in the system.

Password Check

This option enables password checking every time the computer is powered on or every time the BIOS Setup is executed. If ***Always*** is chosen, a user password prompt appears every time the computer is turned on. If ***Setup*** is chosen, the password prompt appears if the BIOS executed.

Boot to OS/2

When using the OS/2 operating system, you need to select ***Yes*** for this option otherwise leave this on the setup default of ***No.***

Wait for 'F1' If Error

AMIBIOS POST error messages are followed by:

```
Press <F1> to continue
```

If this option is set to ***Disabled***, the AMIBIOS does not wait for you to press the <F1> key after an error message.

Hit 'DEL' Message Display

Set this option to ***Disabled*** to prevent the message as follows:

```
Hit 'DEL' if you want to run setup
```

It will prevent the message from appearing on the first BIOS screen when the computer boots.

Internal Cache

This option specifies the caching algorithm used for L1 internal cache memory. The settings are:

Setting	Description
Disabled	Neither L1 internal cache memory on the CPU or L2 secondary cache memory is enabled.
WriteBack	Use the write-back caching algorithm.
WriteThru	Use the write-through caching algorithm.

Internal Cache Setting

System BIOS Cacheable

When this option is set to ***Enabled***, the contents of the F0000h system memory segment can be read from or written to L2 secondary cache memory. The contents of the F0000h memory segment are always copied from the BIOS ROM to system RAM for faster execution.

The settings are ***Enabled*** or ***Disabled***. The <Optimal default settings> is ***Enabled***. The <Fail-Safe default setting> is ***Disabled***.

Shadow

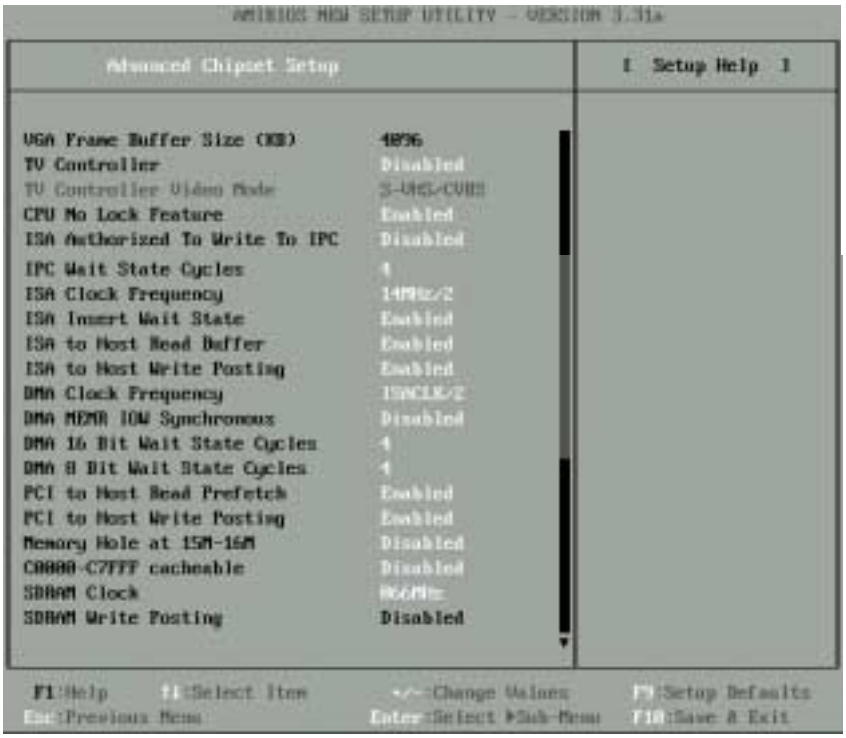
These options control the location of the contents of the 32KB of ROM beginning at the specified memory location. If no adapter ROM is using the named ROM area, this area is made available to the local bus. The settings are:

SETTING	DESCRIPTION
Disabled	The video ROM is not copied to RAM. The contents of the video ROM cannot be read from or written to cache memory.
Enabled	The contents of C000h - C7FFFh are written to the same address in system memory (RAM) for faster execution.
Cached	The contents of the named ROM area are written to the same address in system memory (RAM) for faster execution, if an adapter ROM will be using the named ROM area. Also, the contents of the RAM area can be read from and written to cache memory.

Shadow Setting

5.4 ADVANCED CHIPSET SETUP

This option controls the configuration of the board's chipset. Control keys for this screen are the same as for the previous screen.



Advanced Chipset Setup

VGA Frame Buffer Size

This option sets the VGA's occupied memory size.

Memory Hole at 15-16 MB

This option specifies the range 15MB to 16MB in memory that cannot be addressed on the ISA bus.

ISA Clock Frequency

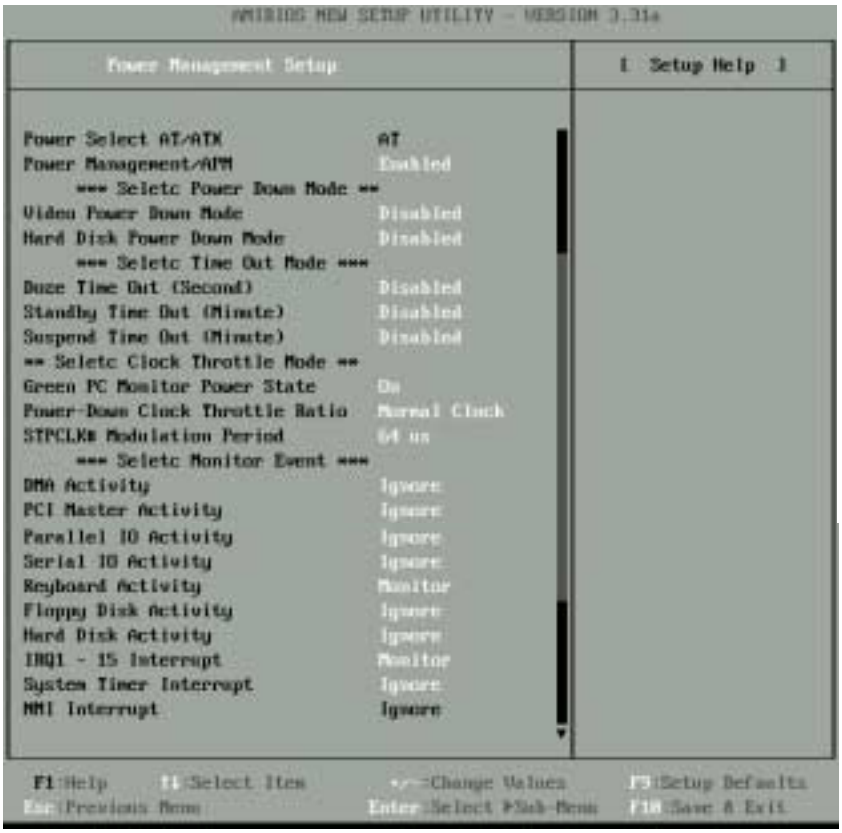
This option is used to select the ISA bus clock rate.

DMA Clock Frequency

This option is used to select the DMA operating clock rate.

5.5 POWER MANAGEMENT

This section is used to configure power management features. This <Power management Setup> option allows you to reduce power consumption. This feature turns off the video display and shuts down the hard disk after a period of inactivity.



Power Management Setup

Power Management /APM

Enabled this option is to enable the power management and APM (Advanced Power Management) features.

Video Power Down Mode

This option specifies the power management states that the video subsystem enters after the specified period of display inactivity have expired.

Hard Disk Power Down Mode

This option specifies the power management states that the hard disk drive enters after the specified period of

display inactivity have expired.

Hard Disk Time Out

This option specifies the length of a period of hard disk inactivity. When this period expired, the hard disk drive enters the power-conserving mode specified on the <Hard Disk Power Down Mode> option.

Standby Time Out

Suspend Time Out

These options specify the length of the period of system inactivity when the computer is already in Standby mode before the computer is placed on Suspend mode. In Suspend mode, nearly all power use is curtailed.

Slow Clock Ratio

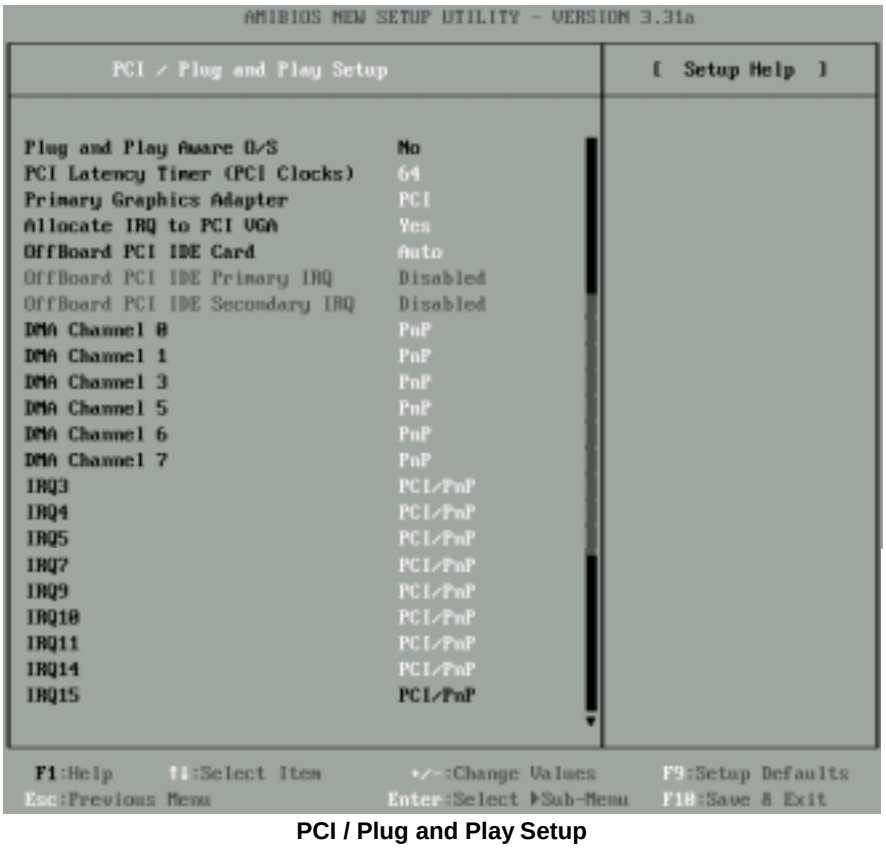
This option specifies the speed at which the system clock runs in power saving modes. The settings are expressed as a ratio between the normal clock speed and the power down clock speed.

IRQ

These options enable event monitoring. When the computer is in a power saving mode, activity on the named interrupt request line is monitored by BIOS. When any activity occurs, the computer enters Full On mode.

5.6 PCI/PLUG AND PLAY

This section is used to configure PCI / Plug and Play features. The <PCI & PNP Setup> option configures the PCI bus slots. All PCI bus slots on the system use INTA#, thus all installed PCI cards must be set to this value.



PCI / Plug and Play Setup

Plug and Play Aware O/S

Set this option to ***Yes*** if the operating system installed in the computer is Plug and Play-aware. The BIOS only detects and enables PnP ISA adapter cards that are required for system boot. The Windows 95 operating system detects and enables all other PnP-aware adapter cards. Windows 95 is PnP-aware. Set this option <***No***> if the operating system (such as DOS, OS/2, Windows 3.x) does not use PnP. You must set this option correctly or PnP-aware adapter cards installed in your computer will not be configured properly.

PCI Latency Timer (PCI Clocks)

This option sets latency of all PCI devices on the PCI bus. The settings are in units equal to PCI clocks.

PCI IDE BusMaster

Enabled this option is to specify that the IDE controller on the PCI local bus has bus mastering capability.

DMA & IRQ

These options specify the bus that the named IRQs/DMAs lines are used on. These options allow you to specify IRQs/DMAs for use by legacy ISA adapter cards. These options determine if the BIOS should remove an IRQ/DMA from the pool of available IRQs/DMAs passed to BIOS configurable devices. If more IRQs/DMAs must be removed from the pool, the end user can use these PCI/PnP Setup options to remove the IRQ/DMA by assigning the option to the ISA/EISA setting. Onboard I/O is configurable by BIOS.

Reserved memory Size

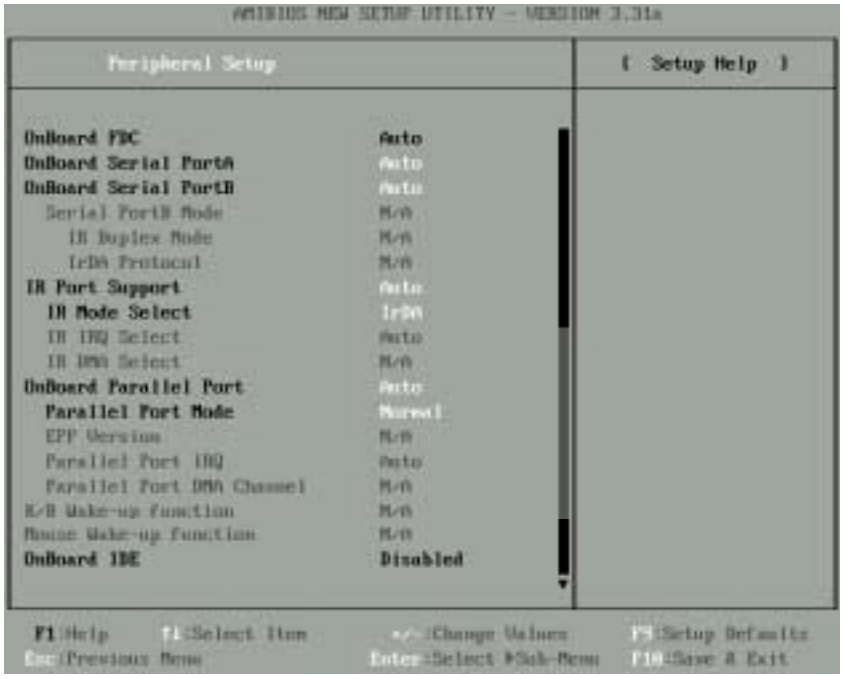
This option specifies the size of the memory area reserved for legacy ISA adapter cards.

Reserved memory Address

This option specifies the beginning address (in hex) of the reserved memory area. The specified ROM memory area is reserved for use by legacy ISA adapter cards.

5.7 PERIPHERAL SETUP

This section is used to configure peripheral features.



Peripheral Setup

OnBoard FDC

This option enables the floppy drive controller on the AR-B1423.

OnBoard Serial Port

This option enables the serial port (COM1& COM2) on the AR-B1423.

OnBoard Parallel Port

This option enables the parallel port on the AR-B1423.

Parallel Port Mode

This option specifies the parallel port mode. ECP and EPP are both bi-directional data transfer schemes that adhere to the IEEE 284 specifications.

5.8 PASSWORD SETTING

This BIOS Setup has an optional password feature. The system can be configured so that all users must enter a password every time the system boots or when BIOS Setup is executed. User can set either a Supervisor password or a User password.

Select the appropriate password icon (Supervisor or User) from the Security section of the BIOS Setup main menu. Enter the password and press [Enter]. The screen does not display the characters entered. After the new password is entered, retype the new password as prompted and press [Enter].

If the password confirmation is incorrect, an error message appears. If the new password is entered without error, press [Esc] to return to the BIOS Main Menu. The password is stored in CMOS RAM after BIOS completes. The next time the system boots, you are prompted for the password function is present and is enabled.

```
Enter new supervisor password:
```

5.9 LOAD DEFAULT SETTING

This section permits users to select a group of settings for all BIOS Setup options. You not only can use these items to quickly set system configuration parameters, but also can choose a group of settings that have a better chance of working when the system is having configuration related problems.

5.9.1 Auto Configuration with Optimal Setting

The user can load the optimal default settings for the BIOS. The Optimal default settings are best-case values that should optimize system performance. If CMOS RAM is corrupted, the optimal settings are loaded automatically.

```
Load high performance setting (Y/N) ?
```

5.9.2 Auto Configuration with Fail Safe Setting

The user can load the Fail-Safe BIOS Setup option settings by selecting the Fail-Safe item from the Default section of the BIOS Setup main menu.

The Fail-Safe settings provide far from optimal system performance, but are the most stable settings. Use this option as a diagnostic aid if the system is behaving erratically.

```
Load failsafe settings (Y/N) ?
```

5.10 BIOS EXIT

This section is used to exit the BIOS main menu. After making your changes, you can either save them or exit the BIOS menu and without saving the new values.

5.10.1 Save Settings and Exit

This item is in the <Standard CMOS Setup>, <Advanced CMOS Setup>, <Advanced Chipset Setup> and the new password (if it has been changed) will be stored in the CMOS. The CMOS checksum is calculated and written into the CMOS.

As you select this function, the following message will appear at the center of the screen to assist you to save data to CMOS and Exit the Setup.

```
Save current settings and exit (Y/N) ?
```

5.10.2 Exit Without Saving

When you select this option, the following message will appear at the center of the screen to help to abandon all the modified data and Exit Setup.

```
Quit without saving (Y/N) ?
```

5.11 BIOS UPDATE

The BIOS program instructions are contained within computer chips called FLASH ROMs that are located on your system board. The chips can be electronically reprogrammed, allowing you to upgrade your BIOS firmware without removing and installing chips.

The AR-B1423 provides FLASH BIOS update function for you to easily upgrade newer BIOS version. Please follow the operating steps for updating new BIOS:

Step 1: Turn on your system and don't detect the CONFIG.SYS and AUTOEXEC.BAT files. ***The importance is that the system has to load the HIMEM.SYS on the memory in the CONFIG.SYS file.***

Step 2: Insert the FLASH BIOS diskette into the floppy disk drive.

Step 3: In the MS-DOS mode, you can type the AMIFLASH program.

A:\>FLASH634

Step 4: The screen will show the message as follow:

Enter the BIOS File name from which Flash EPROM will be programmed. The File name must and with a <ENTER> or press <ESC> to exit.

Step 5: And then please enter the file name to the box of <Enter File Name>. And the box of <Message> will show the notice as follow. In the bottom of this window always show the gray statement.

Flash EPROM Programming is going to start. System will not be usable until Programming of Flash EPROM is successfully complete. In case of any error, existing Flash EPROM must be replaced by new program Flash EPROM.

Step 6: As the gray statement, press the <Y> key to updating the new BIOS.
And then the <Message> box will show the <Programming Flash EPROM>, and the gray statement shows <Please Wait>.

Step 7: The BIOS update is successful, the message will show <Flash Update Completed - Pass>.

NOTE: 1. After turn on the computer and the system didn't detect the boot procedure, please press the [F5] key immediately. The system will pass the CONFIG.SYS and AUTOEXEC.BAT files. ***The importance is that the system has to load the HIMEM.SYS on the memory in the CONFIG.SYS file.***

2. The BIOS Flash disk is not the standard accessory. Now the onboard BIOS is the newest BIOS, if user needs adding some functions in the future please contact technical supporting engineers, they will provide the newest BIOS for updating.
3. The file of FLASH634.EXE had to Version 6.34.

Note:
If the content in setting is inconsistent with the CD-ROM, please refer to the setting as the priority.