APCI-SER4

Introduction

The APCI-SER4 is a 32-bit PCI local bus board which provides 4 channels of RS232/422/485 serial communications. It utilises two 85230 Enhanced serial communication controllers. Each channel can be independently configured for asynchronous or synchronous protocols, baud rate and signalling standards. The board supports communication speeds of up to 115kbaud (asynchronous) and 1.8Mbaud (synchronously).

All serial channel signals are routed to a 50 way D-type connector.

Features

- 4 Serial Communications Channels
- Powerful and versatile 85230 Enhanced Serial Communications controllers
- RS232, RS485 and RS422 signal levels supported
- Transmit and Receive FIFO's
- Interrupt facility
- Board Access LED (RED)
- User LED (GREEN)
- Industry Standard I/O via 50 way D-type
- PCI 2.1 Compatible Bus Interface
- Plug and Play software compatible
- CE Compliant design
- Operating temperature range 0 to +70C
- Power Consumption 250mA@+5V, 70mA@+12, 60mA@-12V
- MTBF: 350,014 hours (using generic figures from MIL-HDBK-217F at ground benign)

Getting Started

- Power down your PC system.
- Install the board in a spare PCI Slot (See Installation for CE compliance).
- Power up system with MSDOS.
- Run APCI.EXE (supplied on the utility disk), this will search for the board and check I/O access. If this fails, check board is correctly located.

Warning

This board contains CMOS devices which may be damaged by static electricity. Please ensure anti-static precautions are taken at all times when handling this board. If for any reason this board is returned to Arcom Control Systems, please ensure it is adequately packed to prevent damage during shipment.

Operation

PCI Bus Interface

The PCI bus is a high speed alternative to ISA bus, it has been designed to overcome some of the limitations of ISA bus, and provide faster throughput for I/O intensive peripheral devices. PCI bus also supports Plug and Play configuration which allows the system software to allocate resources during initialisation helping to overcome resource conflicts, which might exist in a system.

The APCI-SER4 uses a single chip PCI bus slave controller which is designed and manufactured by PLX Technology. This device has been designed to fully support the PCI 2.1 specification and provides plug and play software capabilities. During power-up initialisation the PCI BIOS will detect the card and assign a unique I/O address location and interrupt line. This ensures that there are no resource conflicts on the PCI bus. Multiple cards are supported through this mechanism without the need for address decode links.

The PLX device contains a standard type 00H configuration space header. The table below shows the registers within this header which are required for configuration of the APCI-SER4.

Configuration Space Header

Offset	Register Name	Description	Value
00-01H	Vendor ID	ID of PCI device manufacturer	10B5H (PLX Technology)
02-03H	Device ID	ID of PCI device	9050H
18-1BH	Base Address Register	I/O base address assigned to card	0000xxxx
2C-2DH	Subsystem Vendor ID	ID of board manufacturer	13ABH (ARCOM)
2E-2FH	Subsystem ID	ID of Board	0592H (APCI-SER4)
3CH	Interrupt Line	Interrupt line assigned to device	0x

These registers can be accessed using PCI BIOS functions. Please contact Arcoms customer support team (Tel: 01223 412428) for a copy of the PCI BIOS Specification if required.

Enhanced Serial Communication Controllers

The APCI-SER4 contains two 85230 Enhanced Serial Communication Controllers (ESCC), each device provides two full-duplex communication channels. The serial interface lines from these devices are buffered on board by RS232 and RS485/422 devices.

The ESCC is a versatile and powerful device and requires careful initialisation. For this reason it is recommended that the ESCC manufacturers manual is used. This may be obtained by contacting Arcoms customer support team (Tel:01223 412428). It should be noted that these devices are **NOT** compatible with the PC 8250-type UART.

The order in which registers are initialised is important and a register may need to be accessed more than once during initialisation. Unreliable operation may be experienced if short cuts are taken. For examples of basic ESCC initialisation, please refer to the programs on the utility disk.

Each ESCC occupies four I/O locations in the APCI-SER4 indexed I/O map; two consecutive locations per channel. The lower address of each pair is used to select the appropriate register within the device, and to read/write data to the register. The higher address provides direct connection to the receive and transmit data latches.

The internal ESCC registers are accessed using an indexed addressing scheme like the APCI-SER4. The appropriate index must be written each time a register is accessed. Therefore each read/write operation to a register must be preceded with a write to the index register. After a read/write operation the index is reset to 0.

Initialising ESCC Control Registers

The following procedure is required to access the ESCC registers.

1. Write the control register index (for the appropriate channel) to the APCI-SER4 base address.
2. Write the ESCC register index to the APCI-SER4 base+1 address.
3. Write the new data to the APCI-SER4 base+1 address.
4. Repeat steps 2 and 3 for each of the ESCC registers.

Transmitting and Receiving Data

The following tables show the steps required to transmit and receive deta in polled mode from Channel 2.

Transmit Data

Action	Explanation
Write 02H to the Base address	Sets the APCI-SER4 to read register 0 on Channel 2.
Read from Base+1 address	Reads Status
Logically AND the value with 04H	If bit is set the TX buffer is empty and another byte can be sent. If bit is zero continue to read status.
Write 03H to the base address	Sets APCI-SER4 to write to data register on Channel 2.
Write data to be transmitted to Base+1 address	Data is written to the transmit buffer

Receive Data

Action	Explanation
Write 02H to the Base address	Sets the APCI-SER4 to read register 0 on Channel 2.
Read from Base+1 address	Reads Status
Logically AND the value with 01H	If bit is set there is a byte in the receive register. If bit is zero continue to read status.
Write 03H to the base address	Sets APCI-SER4 to read from the data register on Channel 2.
Read from Base+1 address	Data in receive buffer is read

Baud Rates

Each serial channel has a 16-bit baud rate counter which is used for both transmit and receive data operations. In asynchronous mode, the ESCC can use a x16, x32 or x64 clock.

The following table shows some typical baud rates and their time constants, when the x16 mode is selected:

Baud	Time Constant
9600	22
19200	10
38400	4
115200	0

The baud rate counter is set by writing the low byte of the time constant to ESCC register 12 (decimal) and the upper byte to register 13 (decimal). As the board rates shown in the table above all have time constants of less than 256, their upper bytes are all zero.

Interrupts

The APCI-SER4 has one interrupt signal which is routed to an IRQ line during the PCI BIOS initialisation. This interrupt line is expanded on board to provide two interrupt sources. These interrupts are connected to the output signals from the ESCC devices.

An interrupt source register has been provided at index 10H. The interrupt service routine must read this register to determine which device generated the interrupt request. If bit 0 in this register is set (logic '1') Channel 1 or 2 has requested the interrupt, if bit 7 is set Channel 3 or 4 has requested the interrupt all other bits will be zero.

I/O Map

The APCI-SER4 uses an indexed addressing scheme to access the on-board devices and special function registers. Two consecutive I/O locations are required to implement this scheme, the base address is used to set the index value and the base+1 address is used to access the device.

The I/O base address is set by the PCI BIOS during initialisation (refer to the PCI BUS section of this manual for details). A PCI BIOS function call may be used to determine the base address once the system has been initialised. Multiple boards may be used in a system as each will be given a unique I/O address.

Index Registers

Index	Register Name	Read/Write	Comments
00	S1	Read	Channel 1 Status
00	C1	Write	Channel 1 Control
01	D1	Read/Write	Channel 1 Data
02	S1	Read	Channel 2 Status
02	C1	Write	Channel 2 Control
03	D1	Read/Write	Channel 2 Data
04	S1	Read	Channel 3 Status
04	C1	Write	Channel 3 Control
05	D1	Read/Write	Channel 3 Data
06	S1	Read	Channel 4 Status
06	C1	Write	Channel 4 Control
07	D1	Read/Write	Channel 4 Data
08-0F	N/A	N/A	Not Used
10	INT	Read	Interrupt Line Status

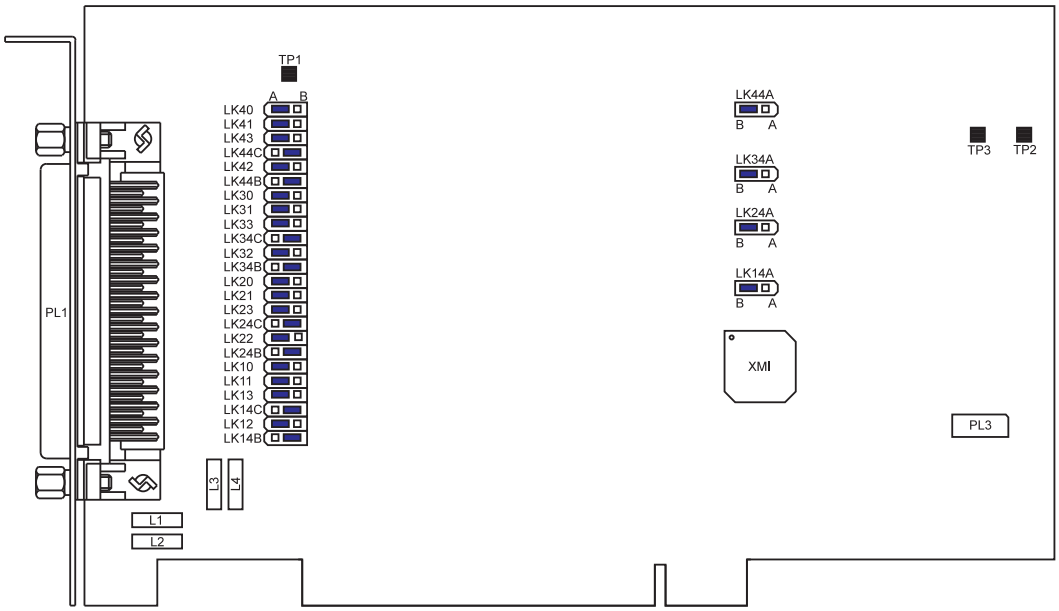
Special Function Registers

Index	Register Name	Read/Write	Comments
80	User LED	Write	01H Switches LED ON 00H Switches LED OFF
81	Board Ident	Read	Always returns 10H for APCI-SER4

Links

Throughout this section a '+' indicates the default link position.

Default Link Positions



There are three functions defined by the links on the APCI-SER4: whether the serial lines are RS232 or RS485/422 (and how some of them are connected); synchronous clock sourcing; and receiver enabling/disabling.

The first digit of the link number refers to the channel i.e LK13 refers to channel 1. The links define whether some of the lines connecting to the ESCC for that channel are at RS232 or RS485/422 levels, and in some cases which lines go to the 50-way connector.

Some of the serial lines are not affected by these links. This is either because they have a connection on the 50-way connector, which is not shared with a different function or level, or because the device can operate at either level.

RS232/485 and RS422 - Serial Signal Connections

Link	Channel	Ribbon Cable Pin No.	A+ Position RS232	B Position RS485/422
LK10	1	9	DTR	DCD–
LK11	1	8	CTS	DTR+
LK12	1	4	TX	TX+
LK13	1	7	RTS	DTR–
LK20	2	19	DTR	DCD–
LK21	2	18	CTS	DTR+
LK22	2	14	TX	TX+
LK23	2	17	RTS	DTR–
LK30	3	29	DTR	DCD–
LK31	3	28	CTS	DTR+
LK32	3	24	TX	TX+
LK33	3	27	RTS	DTR–
LK40	4	39	DTR	DCD–
LK41	4	38	CTS	DTR+
LK42	4	34	TX	TX+
LK43	4	37	RTS	DTR–

Synchronous Clock selection, RS232 and RS485/422 enabling/disabling

There are four groups of nine pins: each group contains three two-position links. They are LK14A-C, LK24A-C, LK34A-C and LK44A-C. The first digit of the link number refers to the channel; the letter refers to the function.

The 'A' links control receiver enables. If a link is inserted in position A on one of these links, the receive buffer is enabled when RTS is active. If the link is in position B, the receive buffer is permanently enabled.

The 'B' links change the function of ribbon cable wires 3, 13, 23 and 33. Position A connects to the RS485 transmitted data signal, position B connects to the 85230 TRXC clock inputs via RS232 buffers.

The 'C' links change the function of ribbon cable wires 5, 15, 25 and 35. Position A connects to the RS485 receive data signal, position B connects to the 85230 RTXC clock inputs via RS232 buffers.

LK14A	A	RX buffer enabled when RTS active
LK14A	B+	RX buffer is permanently enabled

LK14B	A	Pin 3 of D-Type connects RS485 TX data
LK14B	B+	Pin 3 of D-Type connects to 85230 TRXC clock input via RS232 buffer

LK14C	A	Pin 5 of D-Type connects to RS485 RX data
LK14C	B+	Pin 5 of D-Type connects to 85230 RTXC clock input via RS232 buffer

LK24A	A	RX buffer enabled when RTS active
LK24A	B+	RX buffer is permanently enabled

LK24B	A	Pin 13 of D-Type connects RS485 TX data
LK24B	B+	Pin 13 of D-Type connects to 85230 TRXC clock input via RS232 buffer

LK24C	A	Pin 15 of D-Type connects to RS485 RX data
LK24C	B+	Pin 15 of D-Type connects to 85230 RTXC clock input via RS232 buffer

LK34A	A	RX buffer enabled when RTS active
LK34A	B+	RX buffer is permanently enabled

LK34B	A	Pin 23 of D-Type connects RS485 TX data
LK34B	B+	Pin 23 of D-Type connects to 85230 TRXC clock input via RS232 buffer

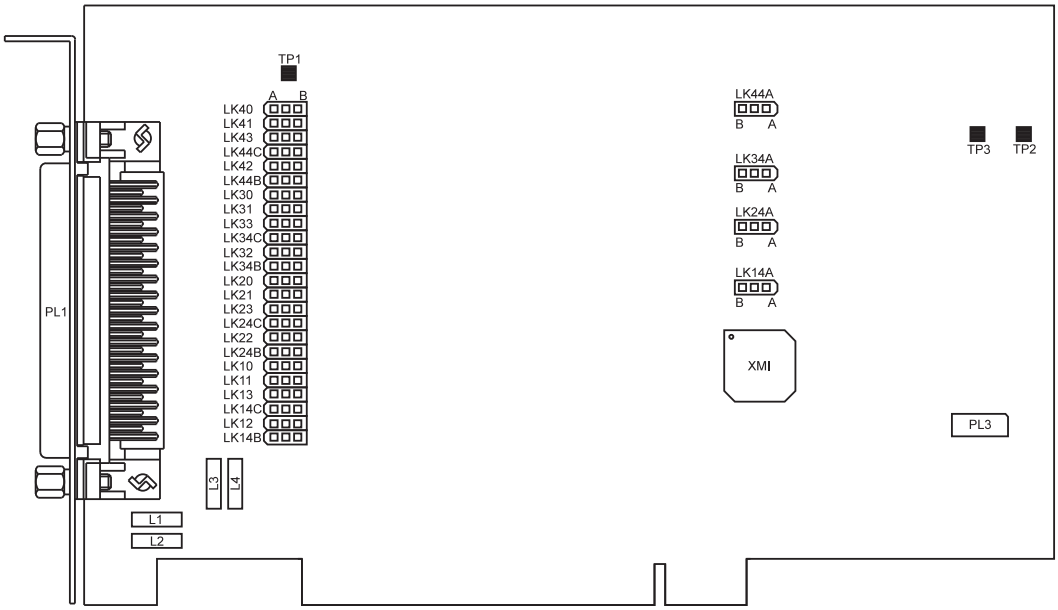
LK34C	A	Pin 25 of D-Type connects to RS485 RX data
LK34C	B+	Pin 25 of D-Type connects to 85230 RTXC clock input via RS232 buffer

LK44A	A	RX buffer enabled when RTS active
LK44A	B+	RX buffer is permanently enabled

LK44B	A	Pin 33 of D-Type connects RS485 TX data
LK44B	B+	Pin 33 of D-Type connects to 85230 TRXC clock input via RS232 buffer

LK44C	A	Pin 35 of D-Type connects to RS485 RX data
LK44C	B+	Pin 35 of D-Type connects to 85230 RTXC clock input via RS232 buffer

User Configuration Record Sheet



Link	Default	User
LK10	A	
LK11	A	
LK12	A	
LK13	A	
LK20	A	
LK21	A	
LK22	A	
LK23	A	
LK30	A	
LK31	A	
LK32	A	
LK33	A	
LK40	A	
LK41	A	
LK42	A	
LK43	A	
LK14A	B	
LK14B	B	
LK14C	B	
LK24A	B	
LK24B	B	
LK24C	B	
LK34A	B	
LK34B	B	
LK34C	B	
LK44A	B	
LK44B	B	
LK44C	B	

D-50 I/O Connector (PL1) Pin Assignments

The pin assignments are listed with the pin number of the D-50 connector and also the pin number when a 50-way IDC ribbon cable is connected to the D-50. The pin assignments conform to the Arcom signal conditioning system (SCS) and may be connected to an external signal conditioning board.

Ribbon Cable Pin No.	D-Type Pin No.	RS232 Signal Name	RS485/RS422 Signal Name	Ribbon Cable Pin No.	D-Type Pin No.	RS232 Signal Name	RS485/RS422 Signal Name
1	1	0V	0V	26	42	RX3	RXA3
2	34	0V	0V	27	26	RTS3	DTRB3
3	18	N/C	TXB1	28	10	CTS3	DTRA3
4	2	TX1	TXA1	29	43	DTR3	DCDB3
5	35	N/C	RXB1	30	27	DCD3	DCDA3
6	19	RX1	RXA1	31	11	0V	0V
7	3	RTS1	DTRB1	32	44	SEE LK34	SEE LK34
8	36	CTS1	DTRA1	33	28	N/C	TXB4
9	20	DTR1	DCDB1	34	12	TX4	TXA4
10	4	DCD1	DCDA1	35	45	N/C	RXB4
11	37	0V	0V	36	29	RX4	RXA4
12	21	SEE LK14	SEE LK14	37	13	RTS4	DTRB4
13	5	N/C	TXB2	38	46	CTS4	DTRA4
14	38	TX2	TXA2	39	30	DTR4	DCDB4
15	22	N/C	RXB2	40	14	DCD4	DCDA4
16	6	RX2	RXA2	41	47	0V	0V
17	39	RTS2	DTRB2	42	31	SEE LK44	SEE LK44
18	23	CTS2	DTRA2	43	15	N/C	N/C
19	7	DTR2	DCDB2	44	48	N/C	N/C
20	40	DCD2	DCDA2	45	32	N/C	N/C
21	24	0V	0V	46	16	N/C	N/C
22	8	SEE LK24	SEE LK24	47	49	-12V	-12V
23	41	N/C	TXB3	48	33	+12V	+12V
24	25	TX3	TXA3	49	17	+5V	+5V
25	9	N/C	RXB3	50	50	+5V	+5V

Installation for CE Compliance

To maintain compliance with the requirements of the EMC directive (89/336/EEC), this product must be correctly installed. The PC system in which the board is housed must be CE compliant as declared by the manufacturer. The type of external I/O cable required can be chosen according to the notes below:

1. Remove the cover of the PC observing any additional instructions of the PC manufacturer.
2. Locate the board in a spare PCI slot and press gently but firmly into place.
3. Ensure that the metal bracket attached to the board is fully seated.
4. fit the bracket clamping screw and firmly tighten this on the bracket.

Note:- Good contact of the bracket to the chassis is essential.

5. Replace the cover of the PC observing any additional instructions of the PC manufacturer.

Cable

Cable length 1 Metre or less	:	Ribbon cable satisfactory.
Cable 1 Metre to 3 Meters	:	Commercial screened cable.
> 3 Meters or noisy environment	:	Use fully screened cable with metal backshells e.g. Arcom CAB50CE

The following standards have been applied to this product:

BS EN50081-1 :	1992 Generic Emissions Standard, Residential, Commercial, Light Industry
BS EN50082-1 :	1992 Generic Immunity Standard, Residential, Commercial, Light Industry
BSEN55022 :	1995 ITE Emissions, Class B, Limits and Methods.

Product Information

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Issue A	V1 Iss 1	980313 First released in this format.